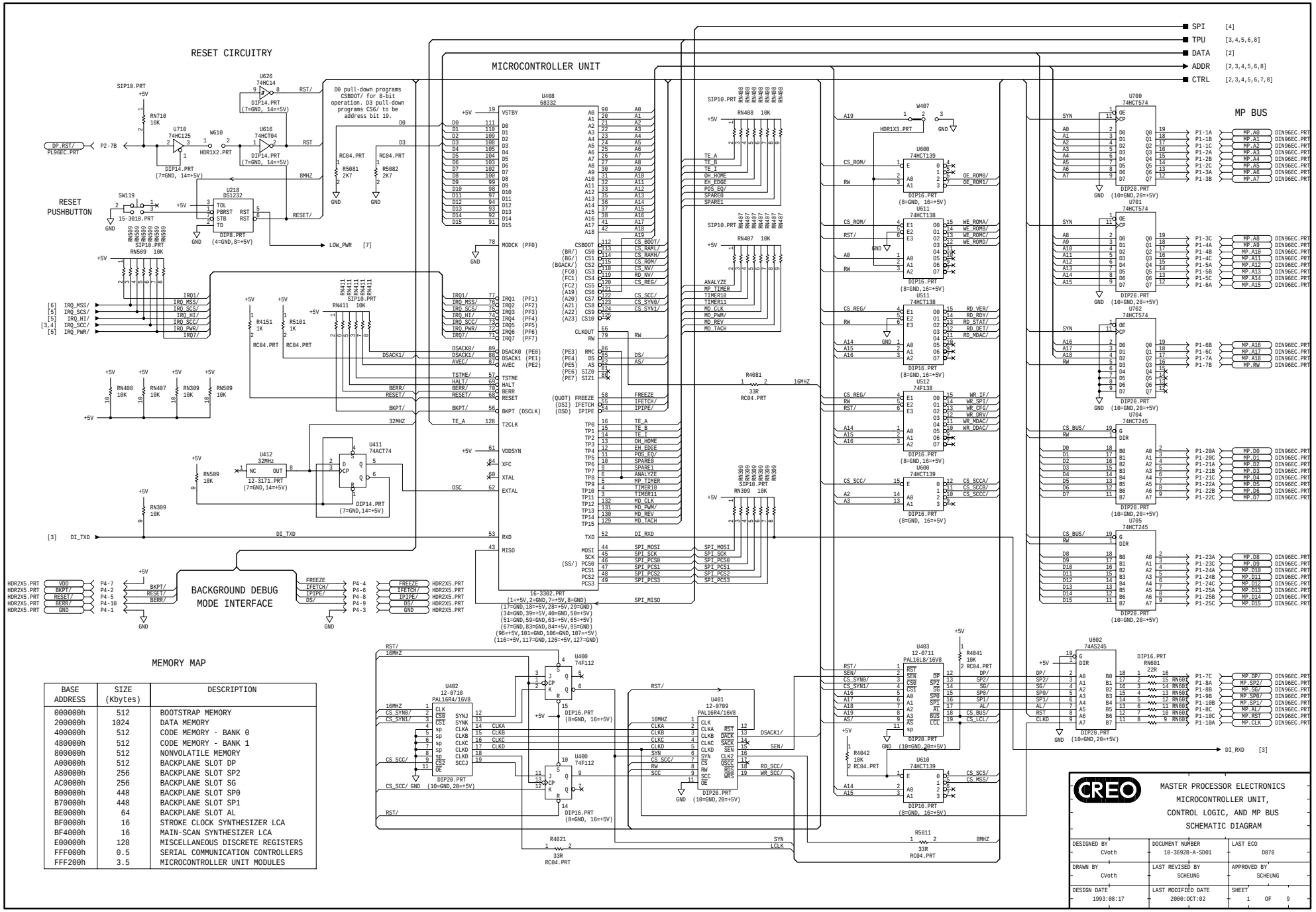
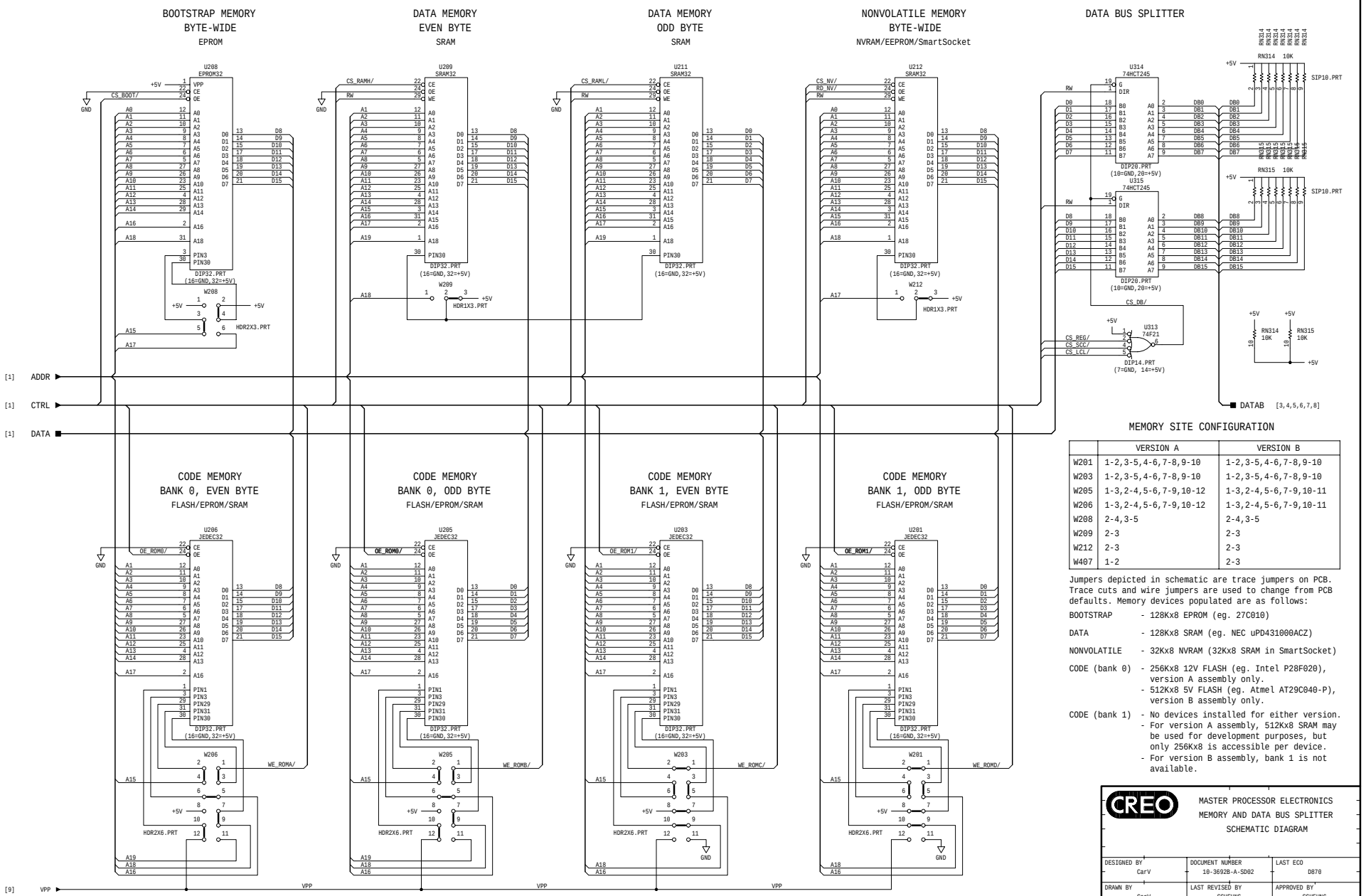


BASE ADDRESS	SIZE (Kbytes)	DESCRIPTION
000000h	512	BOOTSTRAP MEMORY
200000h	1024	DATA MEMORY
400000h	512	CODE MEMORY - BANK 0
480000h	512	CODE MEMORY - BANK 1
800000h	512	NONVOLATILE MEMORY
A00000h	512	BACKPLANE SLOT DP
A80000h	256	BACKPLANE SLOT SP2
AC0000h	256	BACKPLANE SLOT SG
B00000h	448	BACKPLANE SLOT SP0
B70000h	448	BACKPLANE SLOT SP1
BE0000h	64	BACKPLANE SLOT AL
BF0000h	16	STROKE CLOCK SYNTHESIZER LCA
BF4000h	16	MAIN-SCAN SYNTHESIZER LCA
E00000h	128	MISCELLANEOUS DISCRETE REGISTERS
FFF000h	0.5	SERIAL COMMUNICATION CONTROLLERS
FFF200h	3.5	MICROCONTROLLER UNIT MODULES

CREO

MASTER PROCESSOR ELECTRONICS
MICROCONTROLLER UNIT,
CONTROL LOGIC, AND MP BUS
SCHEMATIC DIAGRAM

DESIGNED BY	DOCUMENT NUMBER	LAST ECO
CVoth	10-3692B-A-SD01	D870
DRAWN BY	LAST REVISED BY	APPROVED BY
CVoth	SCHEUNG	SCHEUNG
DESIGN DATE	LAST MODIFIED DATE	SHEET
1993:08:17	2000:OCT:02	1 OF 9



MEMORY SITE CONFIGURATION

	VERSION A	VERSION B
W201	1-2,3-5,4-6,7-8,9-10	1-2,3-5,4-6,7-8,9-10
W203	1-2,3-5,4-6,7-8,9-10	1-2,3-5,4-6,7-8,9-10
W205	1-3,2-4,5-6,7-9,10-12	1-3,2-4,5-6,7-9,10-11
W206	1-3,2-4,5-6,7-9,10-12	1-3,2-4,5-6,7-9,10-11
W208	2-4,3-5	2-4,3-5
W209	2-3	2-3
W212	2-3	2-3
W407	1-2	2-3

Jumpers depicted in schematic are trace jumpers on PCB. Trace cuts and wire jumpers are used to change from PCB defaults. Memory devices populated are as follows:

BOOTSTRAP - 128Kx8 EPROM (eg. 27C010)

DATA - 128Kx8 SRAM (eg. NEC uPD431000ACZ)

NONVOLATILE - 32Kx8 NVRAM (32Kx8 SRAM in SmartSocket)

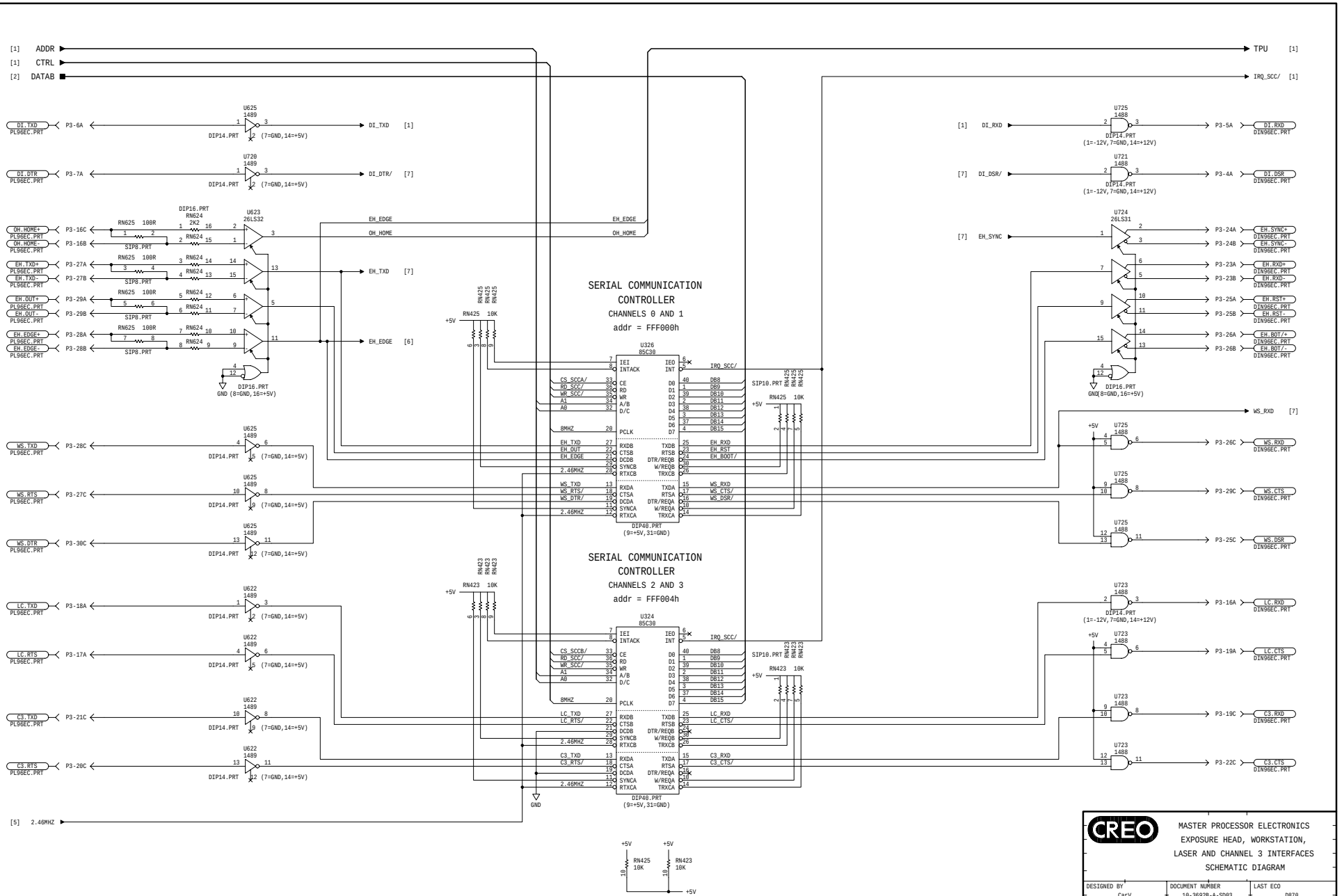
CODE (bank 0) - 256Kx8 12V FLASH (eg. Intel P28F020), version A assembly only.
- 512Kx8 5V FLASH (eg. Atmel AT29C040-P), version B assembly only.

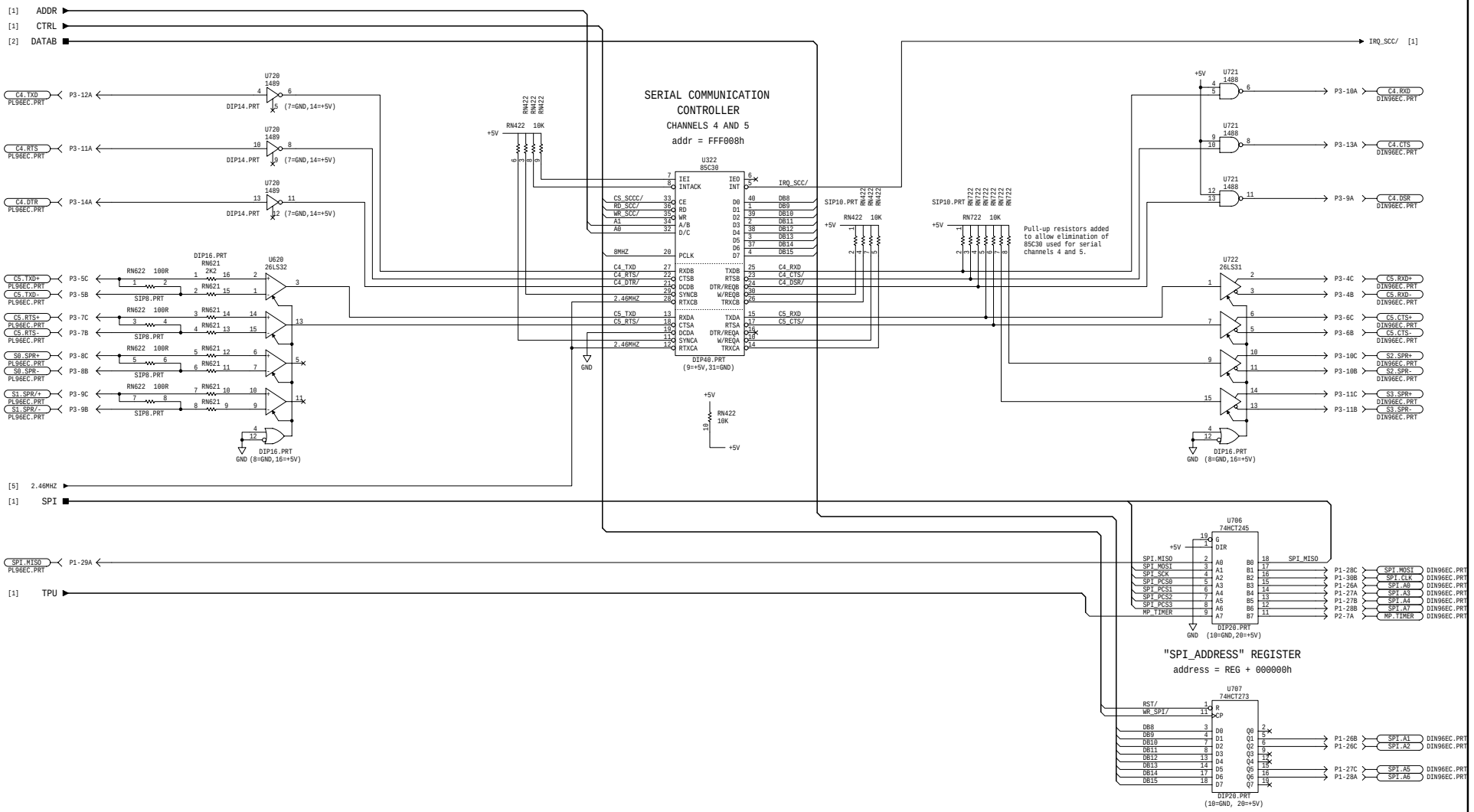
CODE (bank 1) - No devices installed for either version.
- For version A assembly, 512Kx8 SRAM may be used for development purposes, but only 256Kx8 is accessible per device.
- For version B assembly, bank 1 is not available.

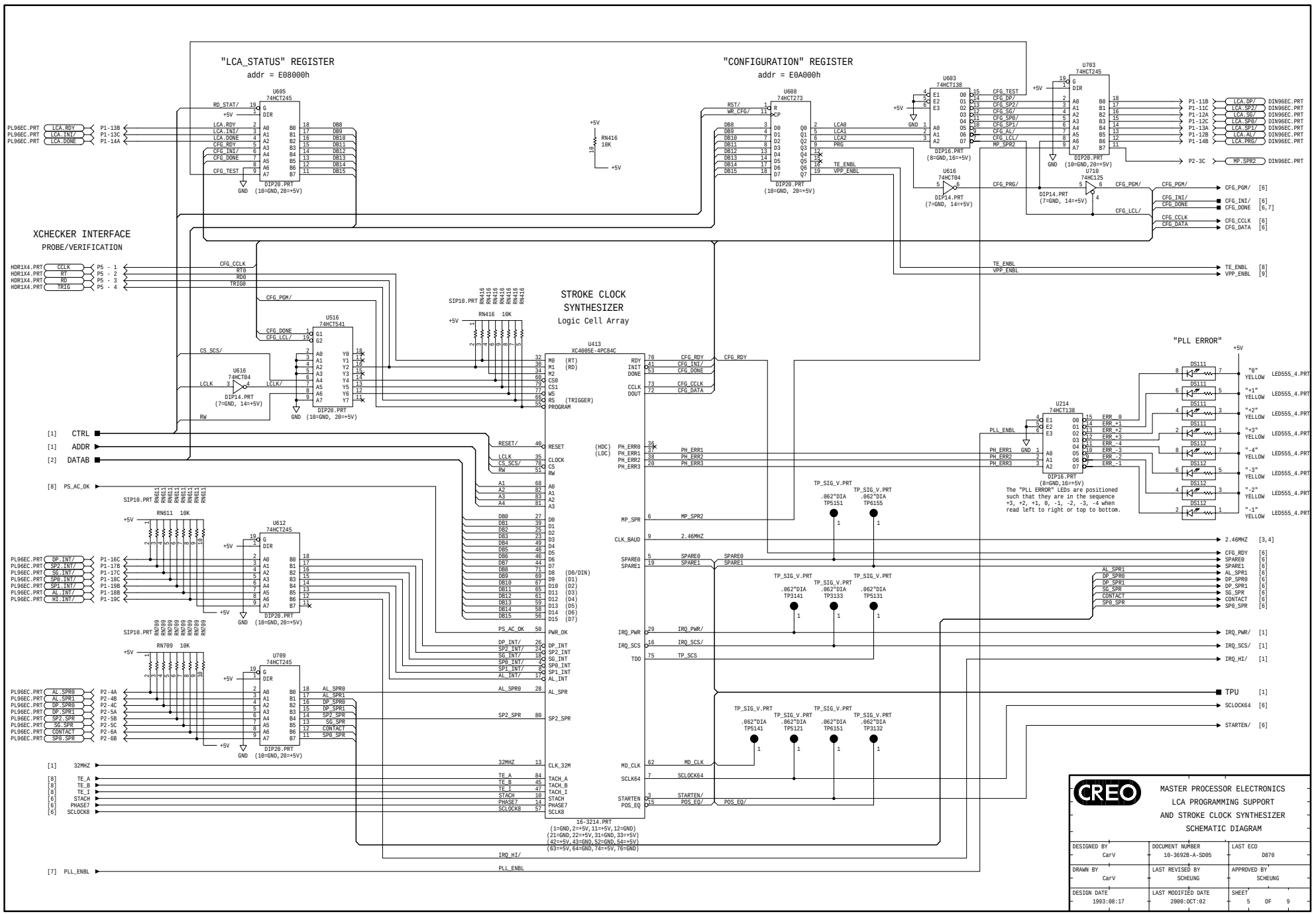
CREO

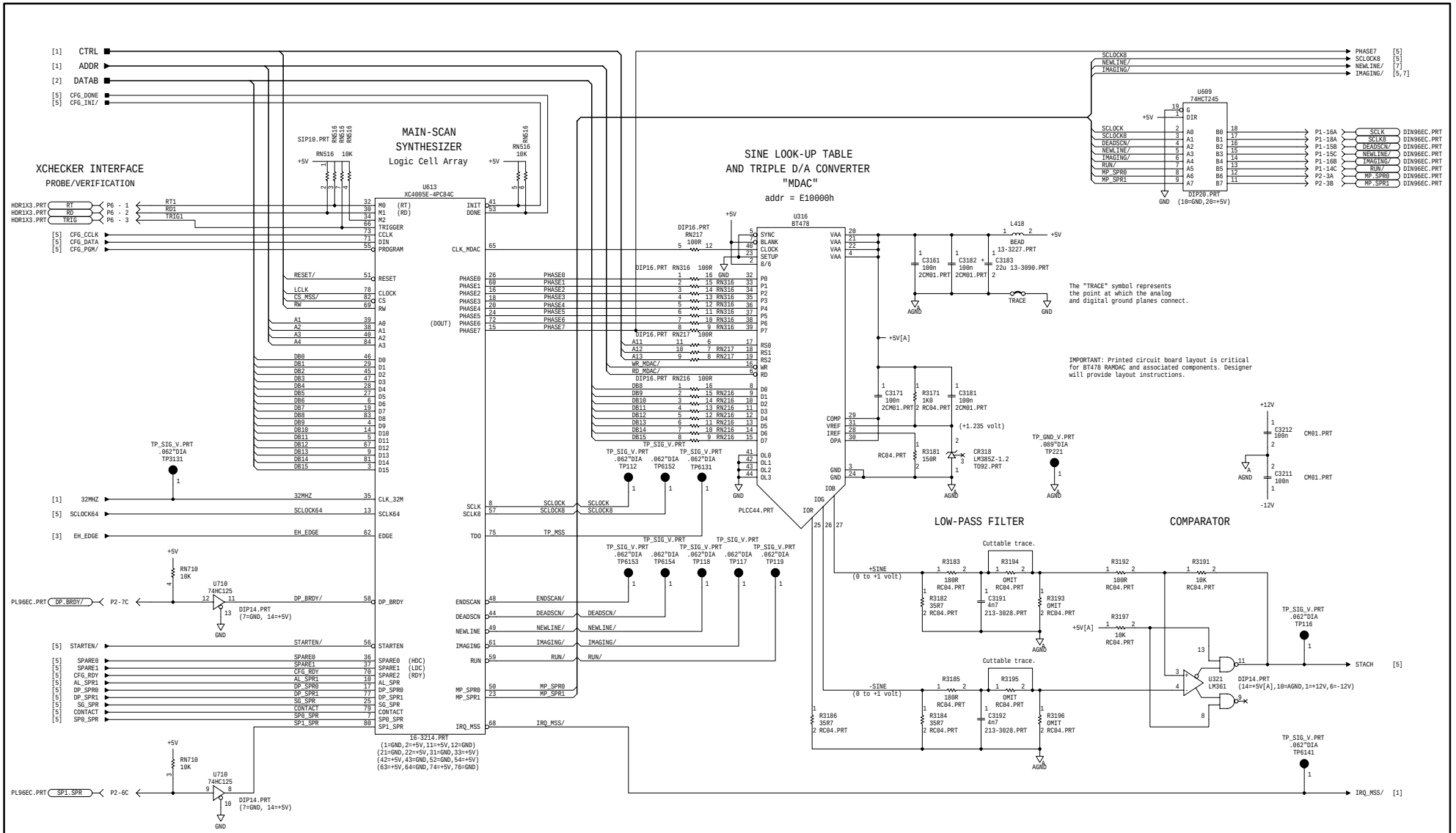
MASTER PROCESSOR ELECTRONICS
MEMORY AND DATA BUS SPLITTER
SCHEMATIC DIAGRAM

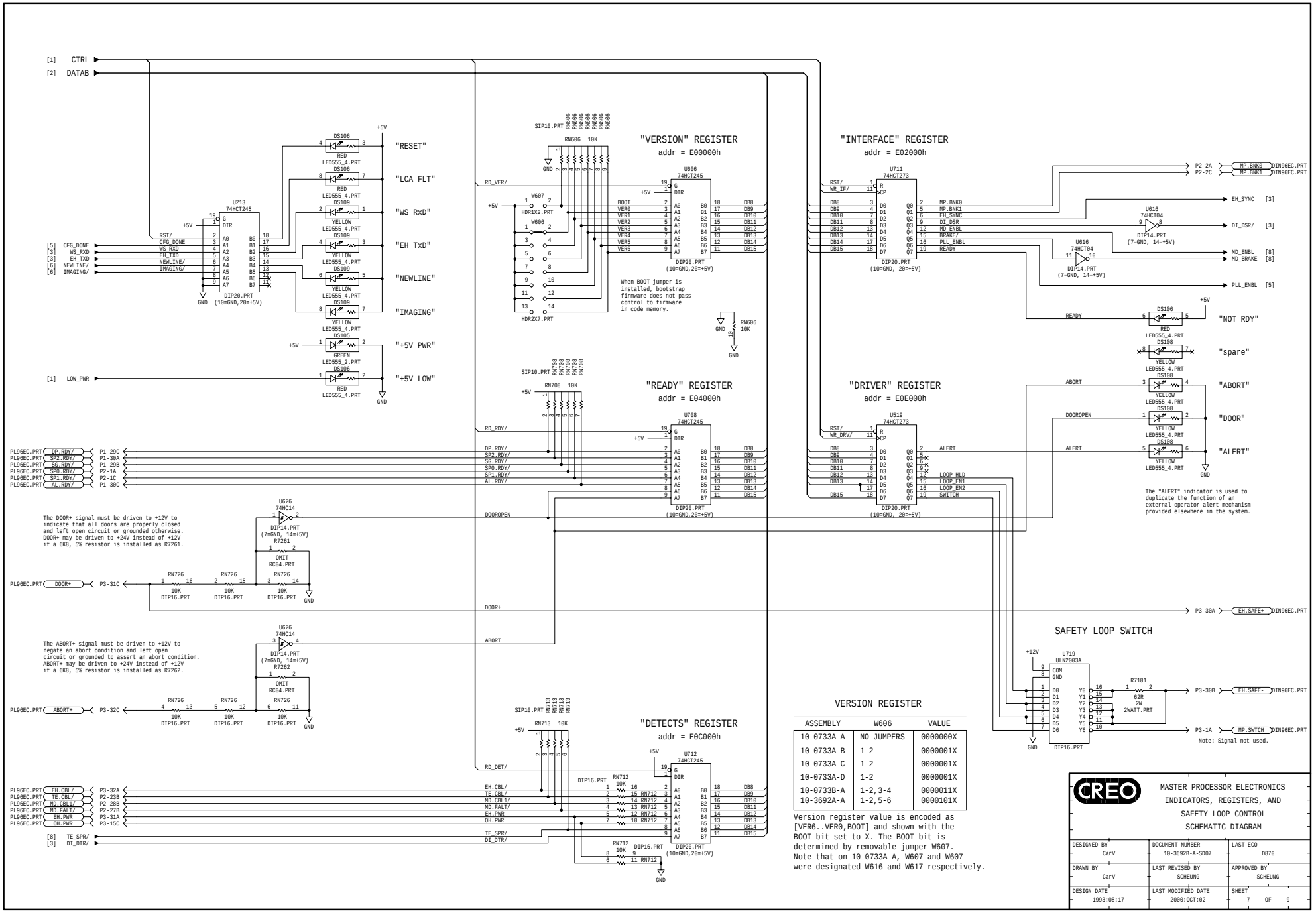
DESIGNED BY: CarV	DOCUMENT NUMBER: 10-3692B-A-SD02	LAST ECO: D870
DRAWN BY: CarV	LAST REVISED BY: SCHEUNG	APPROVED BY: SCHEUNG
DESIGN DATE: 1993:08:17	LAST MODIFIED DATE: 2000:0CT:02	SHEET: 2 OF 9


[1] ADDR
[1] CTRL
[2] DATAB
TPU [1]
IRQ_SCC/ [1]
SERIAL COMMUNICATION CONTROLLER
CHANNELS 0 AND 1
addr = FFF000h
SERIAL COMMUNICATION CONTROLLER
CHANNELS 2 AND 3
addr = FFF004h
U326 85C30
U324 85C30
DIP40.PRT (9=+5V,31=GND)
DIP16.PRT GND (8=GND,16=+5V)
DIP14.PRT (1=-12V,7=GND,14=+12V)
SIP10.PRT
SIP8.PRT
RN425 10K
RN423 10K
DI.TXD
DI.DTR
OH.HOME+
OH.HOME-
EH.TXD+
EH.TXD-
EH.OUT+
EH.OUT-
EH.EDGE+
EH.EDGE-
WS.TXD
WS.RTS
WS.DTR
LC.TXD
LC.RTS
C3.TXD
C3.RTS
DI.RXD
DI.DSR
EH.SYNC+
EH.SYNC-
EH.RXD+
EH.RXD-
EH.RST+
EH.RST-
EH.BDT/+
EH.BDT/-
WS.RXD
WS.CTS
WS.DSR
LC.RXD
LC.CTS
C3.RXD
C3.CTS
[5] 2.46MHZ
CREO
MASTER PROCESSOR ELECTRONICS
EXPOSURE HEAD, WORKSTATION,
LASER AND CHANNEL 3 INTERFACES
SCHEMATIC DIAGRAM
DESIGNED BY CarV
DOCUMENT NUMBER 10-3692B-A-SD03
LAST ECO D870
DRAWN BY CarV
LAST REVISED BY SCHEUNG
APPROVED BY SCHEUNG
DESIGN DATE 1993:08:17
LAST MODIFIED DATE 2000:OCT:02
SHEET 3 OF 9


[1] ADDR
[1] CTRL
[2] DATAB
IRQ_SCC/ [1]
SERIAL COMMUNICATION CONTROLLER
CHANNELS 4 AND 5
addr = FFF008h
U322
85C30
DIP40.PRT
(9=+5V,31=GND)
Pull-up resistors added to allow elimination of 85C30 used for serial channels 4 and 5.
C4.TXD
C4.RTS
C4.DTR
U720
1489
DIP14.PRT
(7=GND,14=+5V)
U721
1488
U722
26LS31
U620
26LS32
DIP16.PRT
GND (8=GND,16=+5V)
C5.TXD+
C5.TXD-
C5.RTS+
C5.RTS-
S0.SPR+
S0.SPR-
S1.SPR/+
S1.SPR/-
RN622 100R
RN621 2K2
SIP8.PRT
RN422 10K
RN722 10K
SIP10.PRT
+5V
GND
8MHZ
2.46MHZ
[5] 2.46MHZ
[1] SPI
[1] TPU
SPI.MISO
P1-29A
U706
74HCT245
DIP20.PRT
(10=GND,20=+5V)
"SPI_ADDRESS" REGISTER
address = REG + 000000h
U707
74HCT273
MASTER PROCESSOR ELECTRONICS
CHANNELS 4 AND 5 INTERFACES
AND SPI INTERFACE
SCHEMATIC DIAGRAM
DESIGNED BY CarV
DOCUMENT NUMBER 10-3692B-A-SD04
LAST ECO D870
DRAWN BY CarV
LAST REVISED BY SCHEUNG
APPROVED BY SCHEUNG
DESIGN DATE 1993:08:17
LAST MODIFIED DATE 2000:OCT:02
SHEET 4 OF 9


"LCA_STATUS" REGISTER
addr = E08000h
"CONFIGURATION" REGISTER
addr = E0A000h
XCHECKER INTERFACE
PROBE/VERIFICATION
STROKE CLOCK SYNTHESIZER
Logic Cell Array
"PLL ERROR"
U605 74HCT245
U608 74HCT273
U603 74HCT138
U703 74HCT245
U710 74HC125
U616 74HCT04
U516 74HCT541
U413 XC4005E-4PC84C
U214 74HCT138
U612 74HCT245
U709 74HCT245
RN416 10K
RN611 10K
RN709 10K
LCA.RDY
LCA.INI/
LCA.DONE
CFG_RDY
CFG_INI/
CFG_DONE
CFG_TEST
CFG_DP/
CFG_SP2/
CFG_SG/
CFG_SP0/
CFG_SP1/
CFG_AL/
CFG_LCL/
MP_SPR2
CFG_PRG/
CFG_PGM/
CFG_CCLK
CFG_DATA
TE_ENBL
VPP_ENBL
CCLK
RT
RD
TRIG
CTRL
ADDR
DATAB
PS_AC_OK
DP.INT/
SP2.INT/
SG.INT/
SP0.INT/
SP1.INT/
AL.INT/
HI.INT/
AL.SPR0
AL.SPR1
DP.SPR0
DP.SPR1
SP2.SPR
SG.SPR
CONTACT
SP0.SPR
32MHZ
TE_A
TE_B
TE_I
STACH
PHASE7
SCLOCK8
PLL_ENBL
IRQ_HI/
IRQ_PWR/
IRQ_SCS/
TP_SCS
TPU
SCLOCK64
STARTEN/
2.46MHZ
CFG_RDY
SPARE0
SPARE1
AL_SPR1
DP_SPR0
DP_SPR1
SG_SPR
CONTACT
SP0_SPR
"0" YELLOW
"+1" YELLOW
"+2" YELLOW
"+3" YELLOW
"-4" YELLOW
"-3" YELLOW
"-2" YELLOW
"-1" YELLOW
The "PLL ERROR" LEDs are positioned such that they are in the sequence +3, +2, +1, 0, -1, -2, -3, -4 when read left to right or top to bottom.
MASTER PROCESSOR ELECTRONICS
LCA PROGRAMMING SUPPORT
AND STROKE CLOCK SYNTHESIZER
SCHEMATIC DIAGRAM
DESIGNED BY CarV
DOCUMENT NUMBER 10-3692B-A-SD05
LAST ECO D870
DRAWN BY CarV
LAST REVISED BY SCHEUNG
APPROVED BY SCHEUNG
DESIGN DATE 1993:08:17
LAST MODIFIED DATE 2000:OCT:02
SHEET 5 OF 9


XCHECKER INTERFACE
PROBE/VERIFICATION
MAIN-SCAN SYNTHESIZER
Logic Cell Array
U613
XC4005E-4PC84C
SINE LOOK-UP TABLE
AND TRIPLE D/A CONVERTER
"MDAC"
addr = E10000h
U316
BT478
U609
74HCT245
DIP20.PRT
(10=GND,20=+5V)
The "TRACE" symbol represents
the point at which the analog
and digital ground planes connect.
IMPORTANT: Printed circuit board layout is critical
for BT478 RAMDAC and associated components. Designer
will provide layout instructions.
LOW-PASS FILTER
COMPARATOR
Cuttable trace.
U321
LM361
DIP14.PRT
(14=+5V[A],10=AGND,1=+12V,6=-12V)
16-3214.PRT
(1=GND,2=+5V,11=+5V,12=GND)
(21=GND,22=+5V,31=GND,33=+5V)
(42=+5V,43=GND,52=GND,54=+5V)
(63=+5V,64=GND,74=+5V,76=GND)
DIP14.PRT
(7=GND, 14=+5V)
PLCC44.PRT
CREO
MASTER PROCESSOR ELECTRONICS
MAIN-SCAN SYNTHESIZER
SCHEMATIC DIAGRAM
DESIGNED BY CarV
DOCUMENT NUMBER 10-3692B-A-SD06
LAST ECO D870
DRAWN BY CarV
LAST REVISED BY SCHEUNG
APPROVED BY SCHEUNG
DESIGN DATE 1993:08:17
LAST MODIFIED DATE 2000:OCT:02
SHEET 6 OF 9



VERSION REGISTER

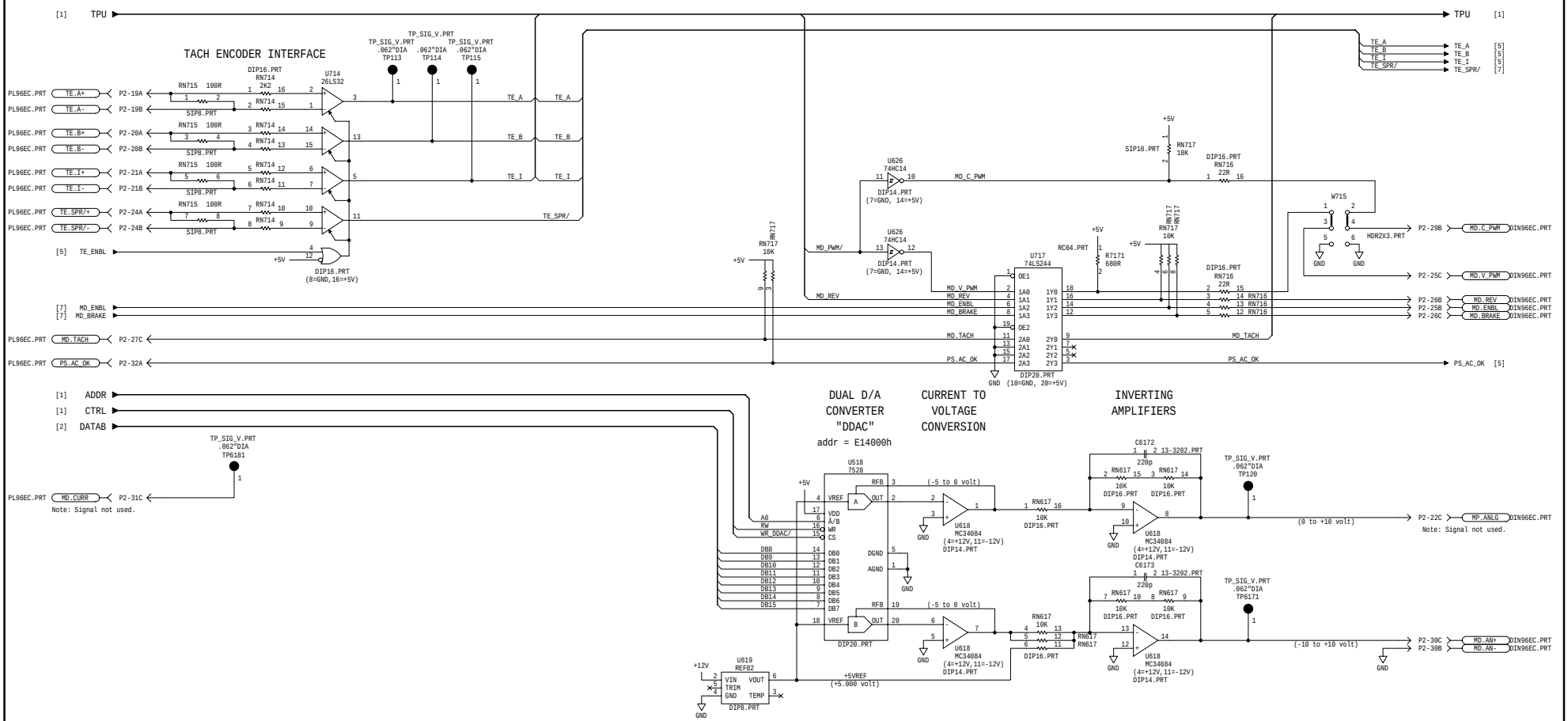
ASSEMBLY	W606	VALUE
10-0733A-A	NO JUMPERS	0000000X
10-0733A-B	1-2	0000001X
10-0733A-C	1-2	0000001X
10-0733A-D	1-2	0000001X
10-0733B-A	1-2,3-4	0000011X
10-3692A-A	1-2,5-6	0000101X

Version register value is encoded as [VER6..VER0,BOOT] and shown with the BOOT bit set to X. The BOOT bit is determined by removable jumper W607. Note that on 10-0733A-A, W607 and W607 were designated W616 and W617 respectively.

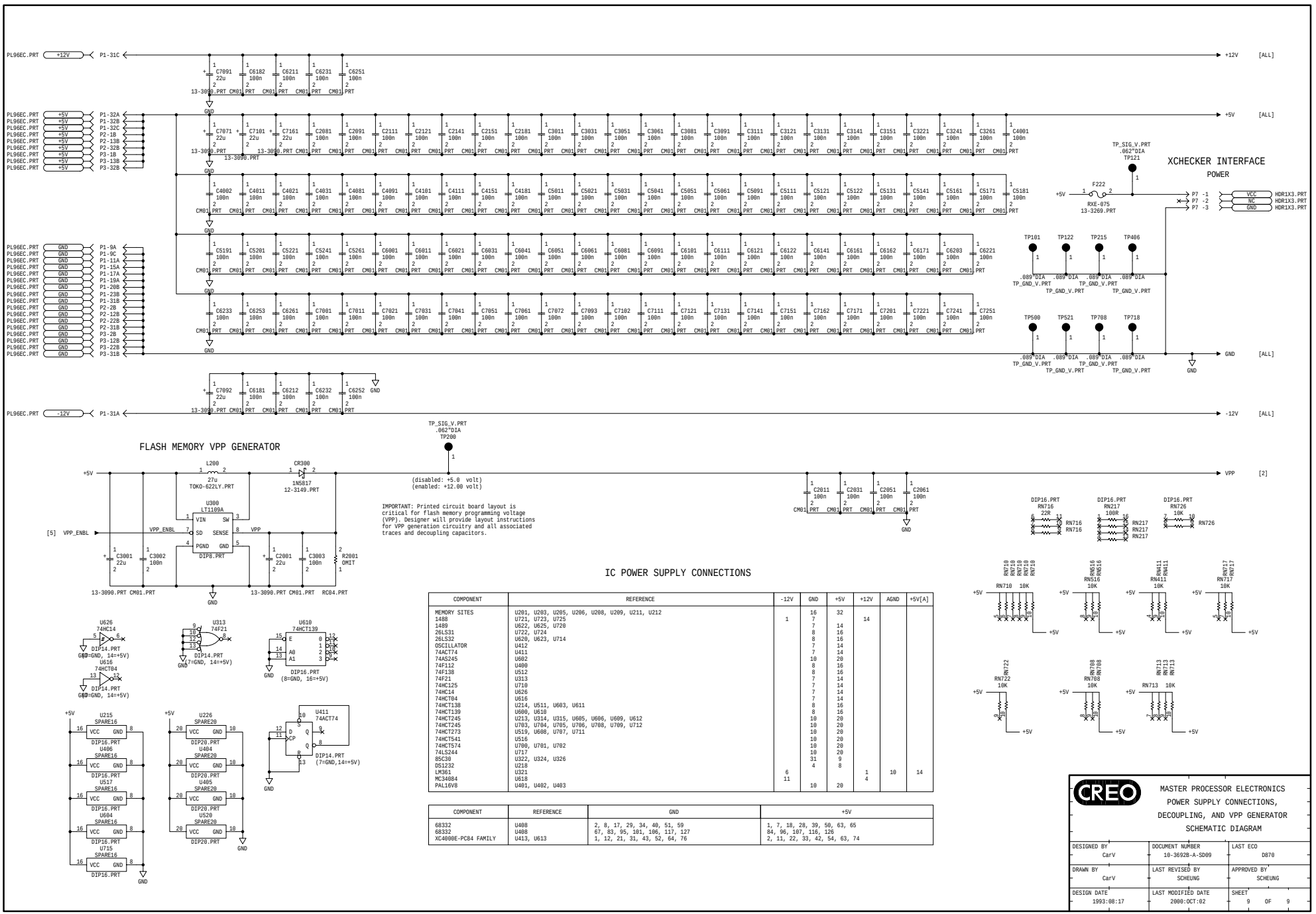
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MASTER PROCESSOR ELECTRONICS
INDICATORS, REGISTERS, AND
SAFETY LOOP CONTROL
SCHEMATIC DIAGRAM

DESIGNED BY: CarV	DOCUMENT NUMBER: 10-3692B-A-SD07	LAST ECO: D870
DRAWN BY: CarV	LAST REVISED BY: SCHEUNG	APPROVED BY: SCHEUNG
DESIGN DATE: 1993:08:17	LAST MODIFIED DATE: 2000:OCT:02	SHEET: 7 OF 9



MASTER PROCESSOR ELECTRONICS TACH ENCODER AND MAIN DRIVE INTERFACES SCHEMATIC DIAGRAM	
DESIGNED BY: CarV	DOCUMENT NUMBER: 10-3692B-A-SD08
DRAWN BY: CarV	LAST REVISED BY: SCHEUNG
DESIGN DATE: 1993:08:17	LAST MODIFIED DATE: 2000:OCT:02
LAST ECO: D870	APPROVED BY: SCHEUNG
	SHEET: 8 OF 9



IC POWER SUPPLY CONNECTIONS

COMPONENT	REFERENCE	-12V	GND	+5V	+12V	AGND	+5V[A]
MEMORY SITES	U201, U203, U205, U206, U208, U209, U211, U212		16	32			
1488	U721, U723, U725	1	7		14		
1489	U622, U625, U720		7	14			
26LS31	U722, U724		8	16			
26LS32	U620, U623, U714		8	16			
OSCILLATOR	U412		7	14			
74ACT74	U411		7	14			
74AS245	U602		10	20			
74F112	U408		8	16			
74F138	U512		8	16			
74F21	U313		7	14			
74HC125	U710		7	14			
74HC14	U626		7	14			
74HCT04	U616		7	14			
74HCT138	U214, U511, U603, U611		8	16			
74HCT139	U600, U610		8	16			
74HCT245	U213, U314, U315, U605, U606, U609, U612		10	20			
74HCT245	U703, U704, U705, U706, U708, U709, U712		10	20			
74HCT273	U519, U608, U707, U711		10	20			
74HCT541	U516		10	20			
74HCT574	U700, U701, U702		10	20			
74LS244	U717		10	20			
85C30	U322, U324, U326		31	9			
DS1232	U218		4	8			
LM361	U321	6			1	10	14
MC34084	U618	11			4		
PAL16V8	U401, U402, U403		10	20			

COMPONENT	REFERENCE	GND	+5V
68332	U408	2, 8, 17, 29, 34, 40, 51, 59	1, 7, 18, 28, 39, 50, 63, 65
68332	U408	67, 83, 95, 101, 106, 117, 127	84, 96, 107, 116, 126
XC4000E-PC84 FAMILY	U413, U613	1, 12, 21, 31, 43, 52, 64, 76	2, 11, 22, 33, 42, 54, 63, 74

CREO

MASTER PROCESSOR ELECTRONICS
POWER SUPPLY CONNECTIONS,
DECOUPLING, AND VPP GENERATOR
SCHEMATIC DIAGRAM

DESIGNED BY: CarV	DOCUMENT NUMBER: 10-3692B-A-SD09	LAST ECO: D870
DRAWN BY: CarV	LAST REVISED BY: SCHEUNG	APPROVED BY: SCHEUNG
DESIGN DATE: 1993:08:17	LAST MODIFIED DATE: 2000:OCT:02	SHEET: 9 OF 9