ADDRESS DECODING

DEVICE ADDRESSES:

VERSION REG.	(RD)	00 - 01
CBL DETECT REG.	(RD)	02 - 03
PWR STATUS REG.	(RD)	04 - 05
EXTERNAL INPUTS	(RD)	06 - 07
PM STATUS REG.	(RD)	08 - 09
PY CONTROLLER	(RD)	0A - 0B
PZ CONTROLLER	(RD)	0C - 0D
ALE OUTPUT REG.	(WR)	40 - 41
CM GAIN DAC	(WR)	42 - 43
CM OFFSET DAC	(WR)	44 - 45
PM CONTROL REG.	(WR)	46 - 47
PY CONTROLLER	(WR)	48 - 49
PZ CONTROLLER	(WR)	4A - 4B
RESET ALE	(WR)	4C - 4D
CM XILINX 0	(R/W)	80 - BF
CM XILINX 1	(R/W)	C0 - FF

DEVICE ADDRESS = 40

NOTE:

MP MUST WRITE TO 0xxx4C WITH D8 CLEARED TO BRING ALE OUT OF RESET.

NOTE:

DATA DIRECTION IS A -> B WHEN DIR IS HIGH.

VERSION REGISTER

NOTE:

ADD JUMPERS TO CHANGE VERSION SIGNATURE

DEVICE ADDRESS = 00

NOTE:

ENABLE SIGNALS INVERTED SO SPARES ARE INACTIVE ON RESET.

INT/ [6]
SPI.MISO [4]

AL.SPR0 [6]
AL.SPR1 [6]

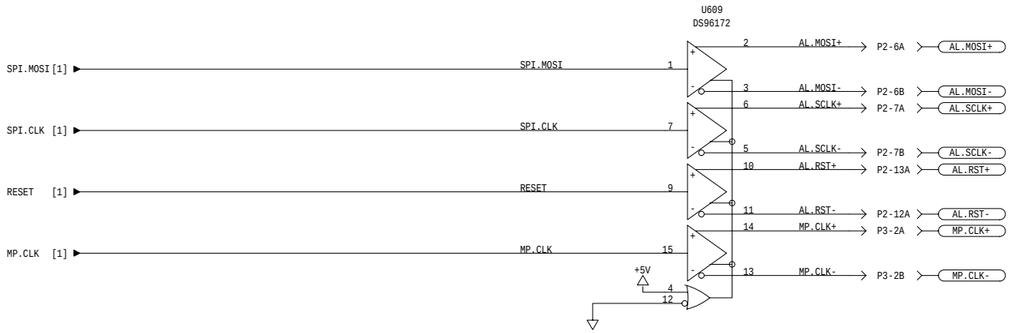
uP CONTROL BUS	
uP ADDRESS BUS	
uP DATA BUS	
SPI ADDRESS BUS	

MASTER PROCESSOR INTERFACE (CTP ALE BOARD)

DESIGNED BY: D.FROESE	DOCUMENT NUMBER: 10-0732C-D-SD01	LAST ECO: A237
DRAWN BY: D.FROESE	LAST REVISED BY: D.FREEMAN	APPROVED BY: R.BOUCHAL
DESIGN DATE: 1993:02:12	LAST MODIFIED DATE: 1996:02:15	SHEET: 1 OF 10

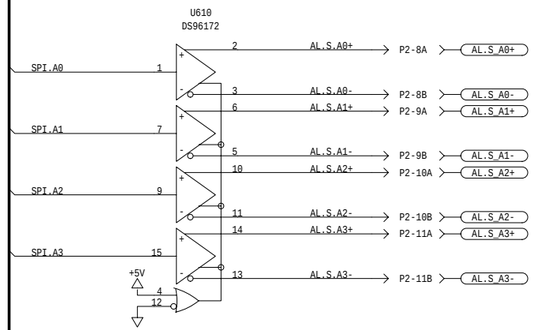
SPI ADDRESS [1]

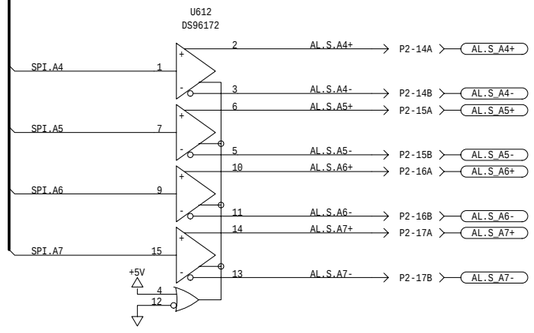
SPI DATA AND SPARE OUTPUTS RS 485 DRIVERS



NOTE: SPI DATA INPUT SIGNAL (MISO) ON PG. 4

SPI ADDRESS BUS RS 485 DRIVERS





SPI BUS INTERFACE (CTP ALE BOARD)

DESIGNED BY	DOCUMENT NUMBER	LAST ECO
D.FROESE	10-0732C-D-SD02	A237
DRAWN BY	LAST REVISED BY	APPROVED BY
D.FROESE	D.FREEMAN	R.BOUCHAL
DESIGN DATE	LAST MODIFIED DATE	SHEET
1993:03:01	1996:02:15	2 OF 10

uP DATA BUS

EXT.RD/ [1]

ALE STATUS AND EXTERNAL INPUTS

PP.Y_HOME+ P2-27C — PP.YHOM+ — U516 DS96173
PP.Y_HOME- P2-27B — PP.YHOM-
PP.Y_AWAY+ P2-29C — PP.YAW+
PP.Y_AWAY- P2-29B — PP.YAW-
PP.Z_HOME+ P2-28C — PP.ZHOM+
PP.Z_HOME- P2-28B — PP.ZHOM-
PP.Z_AWAY+ P2-30C — PP.ZAW+
PP.Z_AWAY- P2-30B — PP.ZAW-
R6171 100R; R617 2K2

PP.SPR_OUT+ P2-30A — PP.SPO+ — U515 DS96173
PP.SPR_OUT- P2-29A — PP.SPO-
LU.QUEUE+ P2-21A — LU.QUE+
LU.QUEUE- P2-22A — LU.QUE-
LU.TE+ P2-23A — LU.TE+
LU.TE- P2-24A — LU.TE-
LU.LDG+ P2-25A — LU.LDG+
LU.LDG- P2-26A — LU.LDG-
R6161 100R; R616 2K2

+5V; R107 10K0

U107 74HCT245 — DEVICE ADDRESS = 06

EXT.RD/	19	G	
	1	DIR	
Y.HOME	2	A0	B0 18 D0
Y.AWAY	3	A1	B1 17 D1
Z.HOME	4	A2	B2 16 D2
Z.AWAY	5	A3	B3 15 D3
PP.SPRIN	6	A4	B4 14 D4
LU.QUEUE	7	A5	B5 13 D5
LU.TE	8	A6	B6 12 D6
LU.LDG	9	A7	B7 11 D7

R505 10K0

U505 74HCT245 — DEVICE ADDRESS = 06

EXT.RD/	19	G	
R406 10K0	1	DIR	
CM.O_CUR	2	A0	B0 18 D8
PY.LIMIT	3	A1	B1 17 D9
SP1.IN1	4	A2	B2 16 D10
PY.FLT	5	A3	B3 15 D11
SP1.CBL/	4	A4	B4 14 D12
SP1.PWR	5	A5	B5 13 D13
	8	A6	B6 12 D14
	9	A7	B7 11 D15

R4061 10K0

CM.O_CUR [8]
PY.LIMIT [4]
SP1.IN1 [4]
PY.FLT [4]

SP1.CBL/ P2-22C — SP1.CBL/
SP1.PWR P2-12C — SP1.PWR

CABLE DETECTS

NOTE:
THIS REGISTER WILL READ 00
IF ALL CABLES ARE PRESENT.

CBL.RD/ [1]

R508 10K0; R507 10K0

U506 74HCT245 — DEVICE ADDRESS = 02

CBL.RD/	19	G	
	1	DIR	
PP.CBL/	1	A0	B0 18 D8
LU.CBL/	2	A1	B1 17 D9
HA.CABL/	3	A2	B2 16 D10
CM.CBL/	4	A3	B3 15 D11
PY.CBL1/	5	A4	B4 14 D12
PY.CBL2/	6	A5	B5 13 D13
	7	A6	B6 12 D14
	8	A7	B7 11 D15

PP.CBL/ P2-32C
LU.CBL/ P2-28A
HA.CBL/ P2-13C
CM.CBL/ P3-1A
PY.CBL1/ P3-1B
PY.CBL2/ P3-1C

NOTE:
CUTTABLE TRACES

TRAILING EDGE CLAMP DETECT INTERRUPT — LU.TE [6]
PLATE QUEUED INTERRUPT — LU.QUEUE [6]

ALE STATUS [5,8,9]

POWER DETECTS

NOTE:
THIS REGISTER WILL READ FF
IF ALL POWER SUPPLIES OK.

PWR.RD/ [1]

R406 10k0

U508 74HCT245 — DEVICE ADDRESS = 04

PWR.RD/	19	G	
	1	DIR	
PP.PWR	1	A0	B0 18 D8
LU.PWR	2	A1	B1 17 D9
CM.PWR	3	A2	B2 16 D10
-2VOK	4	A3	B3 15 D11
-4.5VOK	5	A4	B4 14 D12
-5.2VOK	6	A5	B5 13 D13
+12VOK	7	A6	B6 12 D14
-12VOK	8	A7	B7 11 D15
	9		

PP.PWR P2-31C
LU.PWR P2-27A

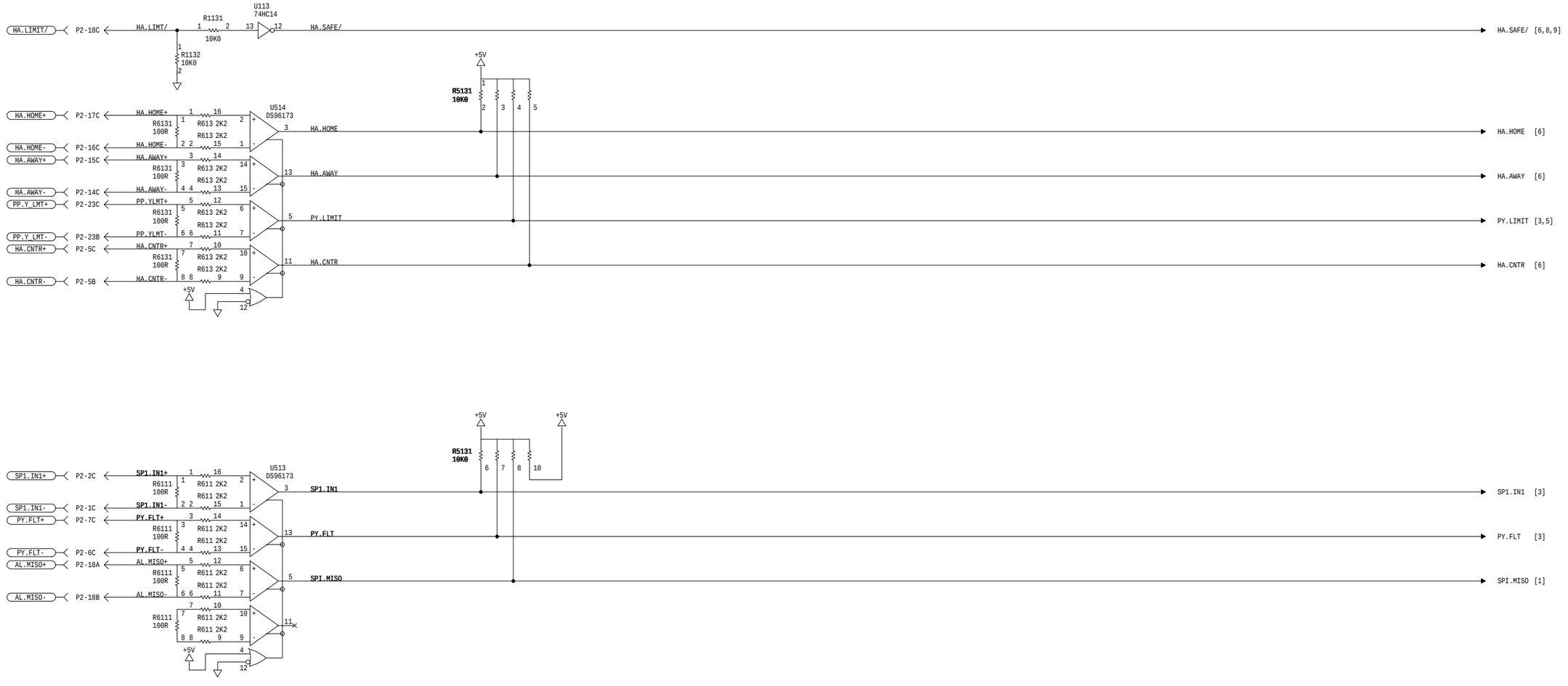
10K0 R4061

CM.PWR [8]
-2VOK [9]
-4.5VOK [9]
-5.2VOK [9]
+12VOK [9]
-12VOK [9]

CREO

INPUT REGISTERS (CTP ALE BOARD)

DESIGNED BY: D.FROESE	DOCUMENT NUMBER: 10-0732C-D-SD03	LAST ECO: A237
DRAWN BY: D.FROESE	LAST REVISED BY: D.FREEMAN	APPROVED BY: R.BOUCHAL
DESIGN DATE: 1993:02:12	LAST MODIFIED DATE: 1996:02:15	SHEET: 3 OF 10



HOME / AWAY BOARD INTERFACE (CTP ALE BOARD)		
DESIGNED BY: D.FROESE	DOCUMENT NUMBER: 10-0732C-D-SD04	LAST ECO: A237
DRAWN BY: D.FROESE	LAST REVISED BY: D.FREEMAN	APPROVED BY: R.BOUCHAL
DESIGN DATE: 1993:02:12	LAST MODIFIED DATE: 1996:02:15	SHEET: 4 OF 10

PICK.RD/ [1]
SP1.OUT1 [1]
PY.LIMIT [4]

PICKER CONTROL REGISTER

U504 74HCT273
RESET/ [1]
PICK.WR/ [1]
DATA BUS [1]
RESET [1]
DEVICE ADDRESS = 46
PY.RESET
PY.REQ
PY.ABORT
PZ.RESET
PZ.REQ
QUEUE.EN
PZ.ABORT

Y.AWAY [3]
Y.HOME [3]
U113 74HC14

PY.WR/ [1]
PY.RD/ [1]

Y-AXIS I/O REGISTER

U510 74HCT74
U511 74HCT652
U410 74HCT32
U113 74HC14
PY.WR/
PY.BUSY/
PY.DATA/
DATA BUS [1]
READ ADDRESS = 0A
WRITE ADDRESS = 48

U409 74HC14
PY.LIMIT
U405 74HCT08
PY.LIMT/
PY.PULSE

PICKER Y-AXIS STEPPER CONTROLLER

U410 74HCT32
RESET
PY.RESET
PY.RXD [5]
U113 74HC14
PY.ABORT
U312 16MHz. CMOS CRYSTAL OSC.
16MHZCLK
PY.REQ

U210 CY545
PY.RXD
PY.RST
PY.AWAY/
PY.HOME/
PY.ABRT/
PY.REQ/
PICY_D0
PICY_D1
PICY_D2
PICY_D3
PICY_D4
PICY_D5
PICY_D6
PICY_D7
PULSE/
CCW
STOPPED
SLEW/
MEM_SEL/
HP_SEL/
SW_SEL/
WR/
RD/
ALE
TXD
FPL/
BUSY/
RESERVED
USRB0
USRB1
USRB2
USRB3
USRB4
USRB5
PY.PULSE
PY.DIR
PY.STOP
PY.TXD
PY.DATA/
PY.BUSY/
PY.HOME/

R2102 10K0
R2101 10K0

U614 DS96172
PY.PLS
PY.DIR
PY.STOP
SP1.OUT1
PY.YPLS+
PY.YPLS-
PY.YDIR+
PY.YDIR-
PY.YSTP+
PY.YSTP-
SP1.OP1+
SP1.OP1-
P2-19C PY.YPULSE+
P2-19B PY.YPULSE-
P2-20C PY.YDIR+
P2-20B PY.YDIR-
P2-21C PY.YSTOP+
P2-21B PY.YSTOP-
P2-9C SP1.OUT1+
P2-8C SP1.OUT1-

PICKER STATUS REGISTER

U512 74HCT245
PICK.RD/
PY.STOP
PY.DIR
PY.DATA/
PY.BUSY/
PZ.STOP
PZ.DIR
PZ.DATA/
PZ.BUSY/
DEVICE ADDRESS = 08
DATA BUS [1]

RS-232 INTERFACE

NOTE: INSTALL THESE PARTS FOR DEVELOPMENT ONLY
J2121
J2122
U112 1488
U408 1489
PY.TXD
PZ.TXD
PY.RXD
PZ.RXD

Z.HOME [3]
LU.QUEUE [3]
U409 74HC14
U405 74HCT08
QUEUE.EN
LU.QUEUE

PICKER Z-AXIS STEPPER CONTROLLER

U406 74HCT32
RESET
PZ.RESET
PZ.RXD [5]
PZ.QUE
PZ.ABORT
PZ.REQ

U208 CY545
PZ.RXD
PZ.RST
PZ.HOME/
PZ.ABRT/
PZ.REQ/
PICKZ_D0
PICKZ_D1
PICKZ_D2
PICKZ_D3
PICKZ_D4
PICKZ_D5
PICKZ_D6
PICKZ_D7
PZ.PULSE
PZ.DIR
PZ.STOP
PZ.TXD
PZ.DATA/
PZ.BUSY/
PZ.HOME/

R2082 10K0

U615 DS96172
PZ.PULSE
PZ.DIR
PZ.STOP
PY.ENBL
PP.ZPLS+
PP.ZPLS-
PP.ZDIR+
PP.ZDIR-
PP.ZSTP+
PP.ZSTP-
PY.ENBL+
PY.ENBL-
P2-24C PP.ZPULSE+
P2-24B PP.ZPULSE-
P2-25C PP.ZDIR+
P2-25B PP.ZDIR-
P2-26C PP.ZSTOP+
P2-26B PP.ZSTOP-
P2-11C PY.ENBL+
P2-10C PY.ENBL-

Z-AXIS I/O REGISTER

U510 74HCT74
U509 74HCT652
U406 74HCT32
U409 74HC14
PZ.WR/
PZ.BUSY/
PZ.DATA/
R2081 10K0
DATA BUS [1]
READ ADDRESS = 0C
WRITE ADDRESS = 4A

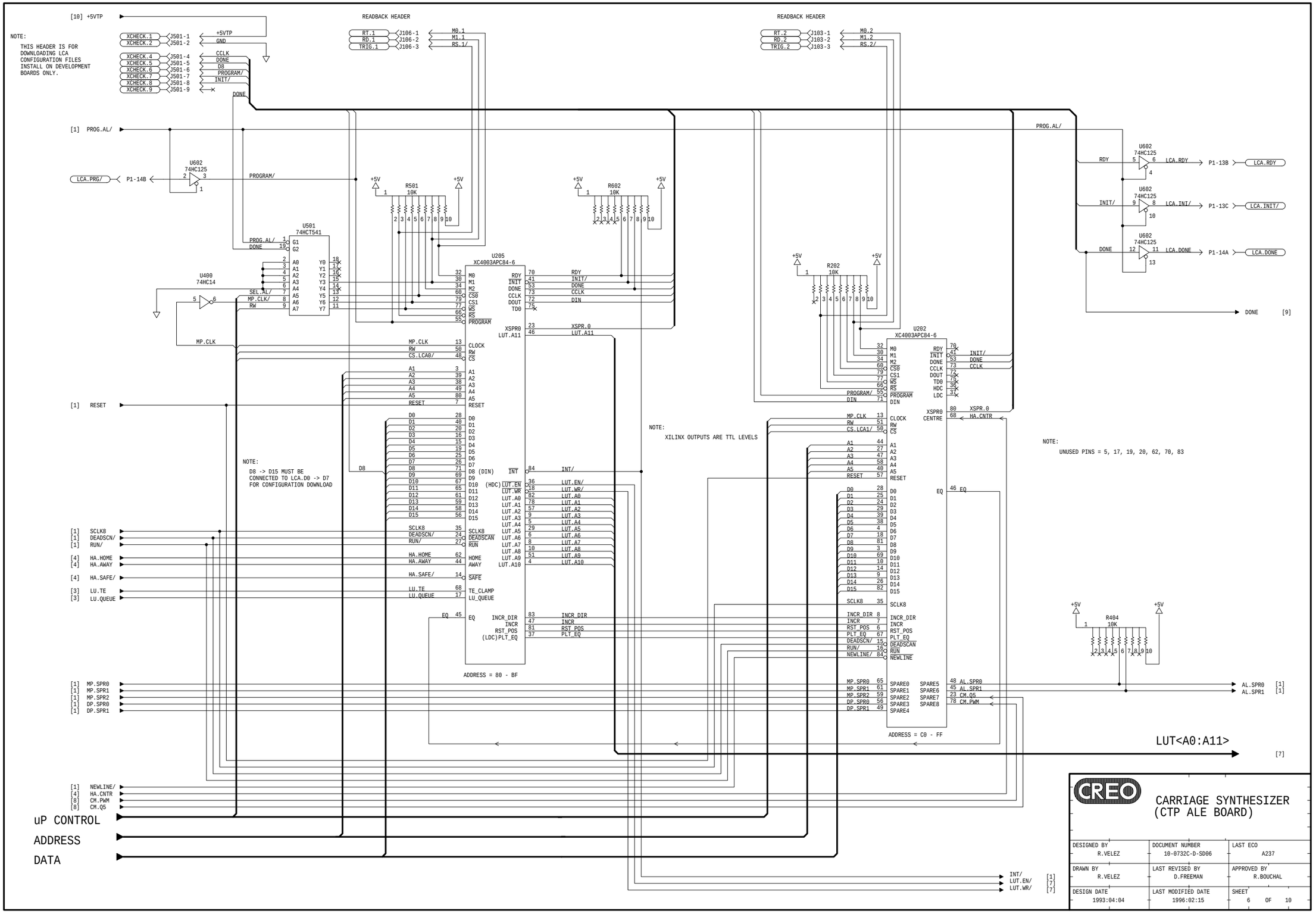
Spare Components
U409 74HC14

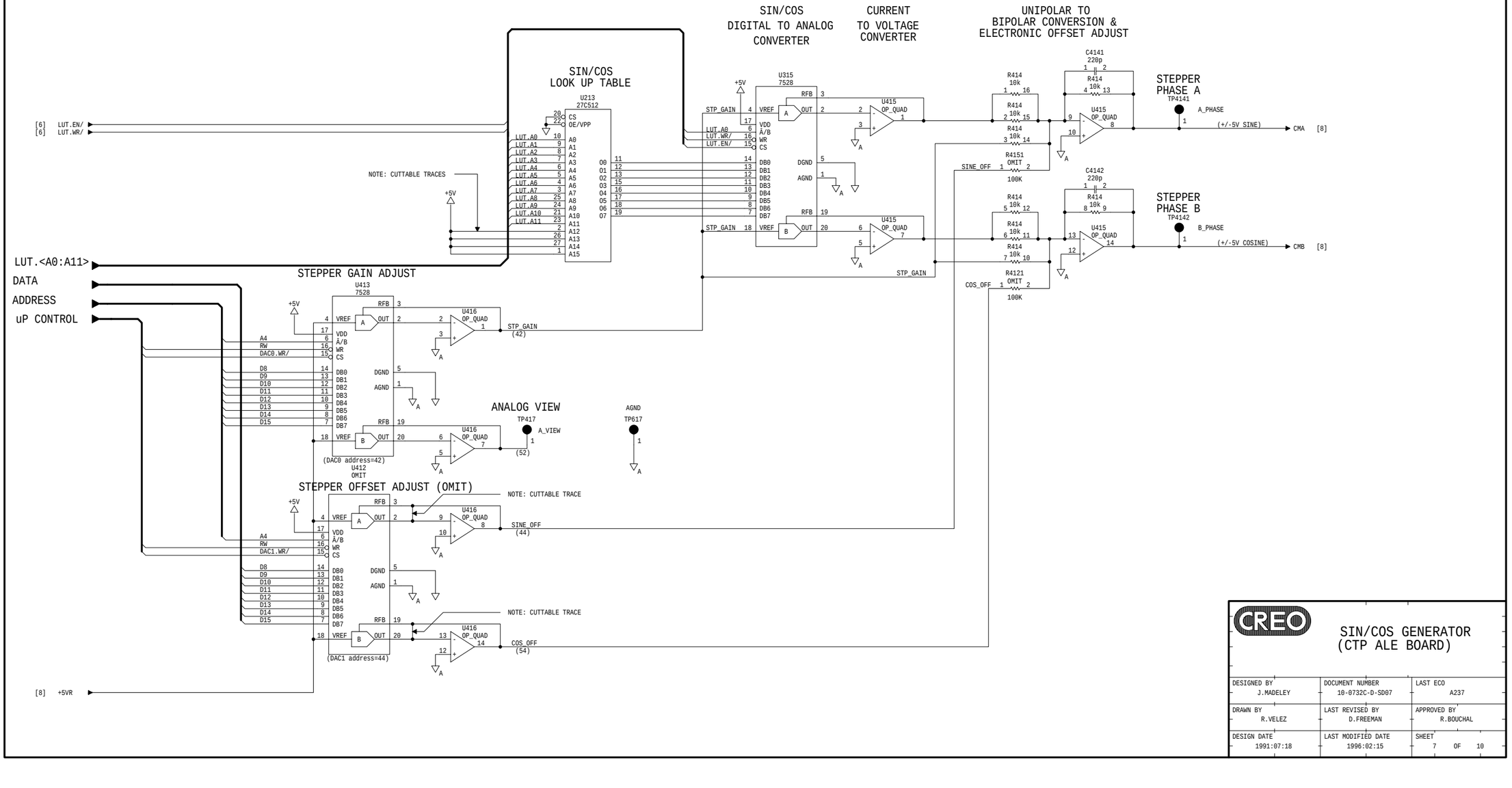
PZ.WR/ [1]
PZ.RD/ [1]
PY.ENBL [1]

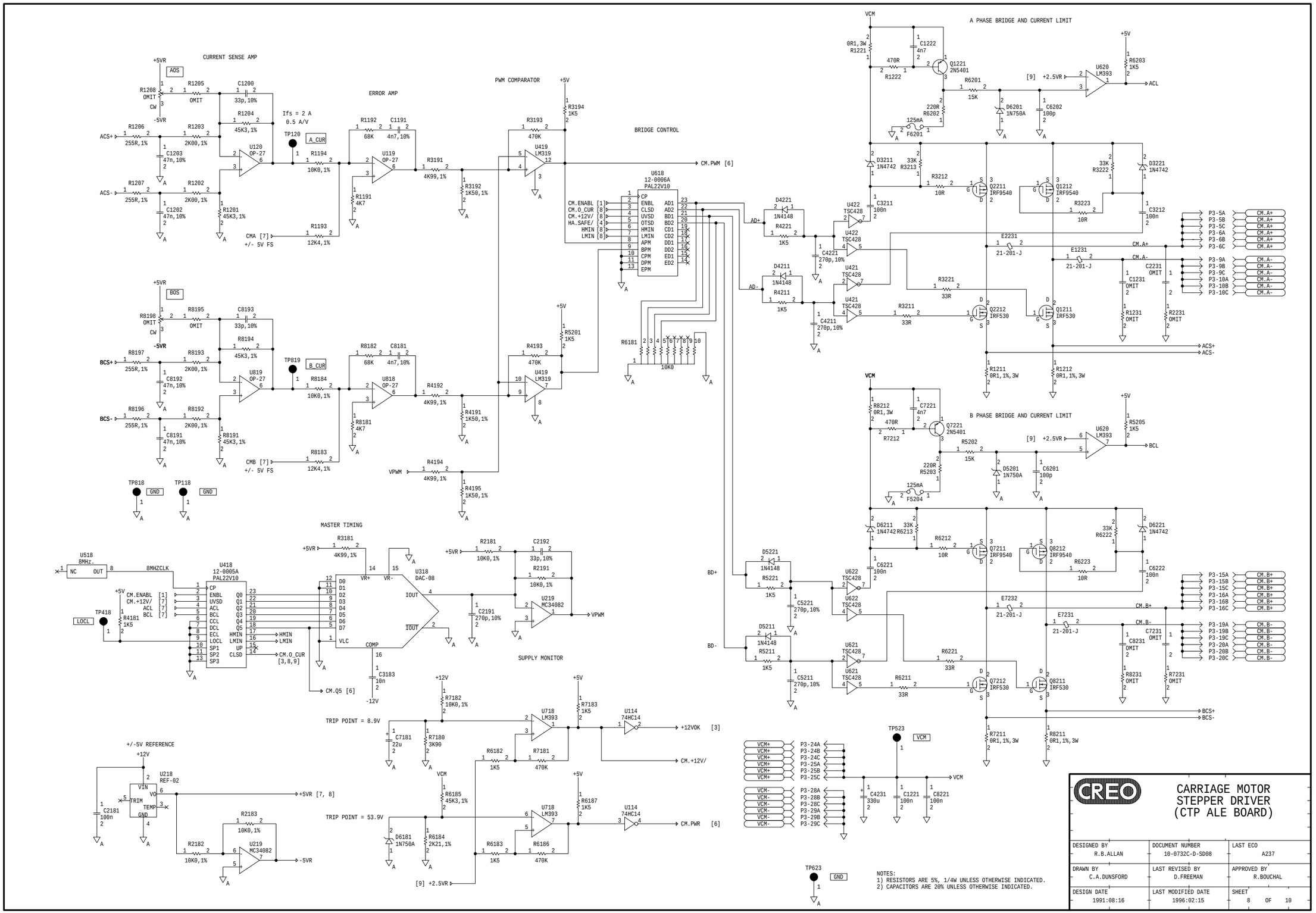
CREO

PICKER STEPPER CONTROLLER (CTP ALE BOARD)

DESIGNED BY: D.FROESE	DOCUMENT NUMBER: 10-0732C-D-SD05	LAST ECO: A237
DRAWN BY: D.FROESE	LAST REVISED BY: D.FREEMAN	APPROVED BY: R.BOUCHAL
DESIGN DATE: 1993;03:29	LAST MODIFIED DATE: 1996:02:15	SHEET: 5 OF 10

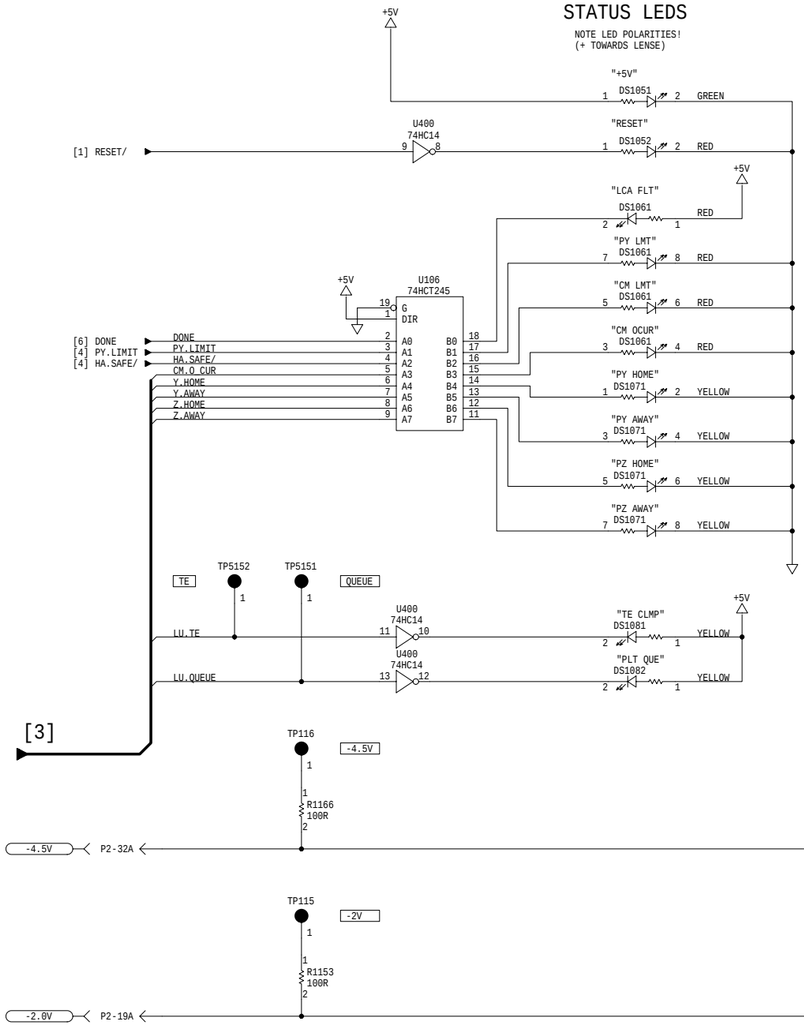

[10] +5VTP
NOTE:
THIS HEADER IS FOR DOWNLOADING LCA CONFIGURATION FILES INSTALL ON DEVELOPMENT BOARDS ONLY.
XCHECK.1 J501-1 +5VTP
XCHECK.2 J501-2 GND
XCHECK.4 J501-4 CCLK
XCHECK.5 J501-5 DONE
XCHECK.6 J501-6 D8
XCHECK.7 J501-7 PROGRAM/
XCHECK.8 J501-8 INIT/
XCHECK.9 J501-9
DONE
READBACK HEADER
RT.1 J106-1 M0.1
RD.1 J106-2 M1.1
TRIG.1 J106-3 RS.1/
READBACK HEADER
RT.2 J103-1 M0.2
RD.2 J103-2 M1.2
TRIG.2 J103-3 RS.2/
[1] PROG.AL/
PROG.AL/
LCA.PRG/ P1-14B
U602 74HC125
PROGRAM/
R501 10K
R602 10K
R202 10K
U501 74HC541
U400 74HC14
U205 XC4003APC84-6
U202 XC4003APC84-6
RDY
INIT/
DONE
CCLK
DOUT
TD0
XSPR0
LUT.A11
PROGRAM/
DIN
MP.CLK
RW
CS.LCA0/
CS.LCA1/
RESET
D0
D1
D2
D3
D4
D5
D6
D7
D8 (DIN)
D9
D10 (HDC)
D11
D12
D13
D14
D15
INT
LUT.EN
LUT.WR
LUT.A0
LUT.A1
LUT.A2
LUT.A3
LUT.A4
LUT.A5
LUT.A6
LUT.A7
LUT.A8
LUT.A9
LUT.A10
SCLK8
DEADSCN/
RUN/
DEADSCAN
RUN
HA.HOME
HA.AWAY
HA.SAFE/
SAFE
LU.TE
LU.QUEUE
TE_CLAMP
LU_QUEUE
EQ
INCR_DIR
INCR
RST_POS
PLT_EQ
(LDC)
NEWLINE/
HA.CNTR
CM.PWM
CM.Q5
MP.SPR0
MP.SPR1
MP.SPR2
DP.SPR0
DP.SPR1
SPARE0
SPARE1
SPARE2
SPARE3
SPARE4
SPARE5
SPARE6
SPARE7
SPARE8
AL.SPR0
AL.SPR1
CM.Q5
CM.PWM
HDC
LDC
CENTRE
R404 10K
NOTE:
D8 -> D15 MUST BE CONNECTED TO LCA.D0 -> D7 FOR CONFIGURATION DOWNLOAD
NOTE:
XILINX OUTPUTS ARE TTL LEVELS
NOTE:
UNUSED PINS = 5, 17, 19, 20, 62, 70, 83
ADDRESS = 80 - BF
ADDRESS = C0 - FF
LCA.RDY
LCA.INIT/
LCA.DONE
LCA.AL0
LCA.AL1
LUT<A0:A11>
uP CONTROL
ADDRESS
DATA
CREO
CARRIAGE SYNTHESIZER
(CTP ALE BOARD)
DESIGNED BY R.VELEZ
DOCUMENT NUMBER 10-0732C-D-SD06
LAST ECO A237
DRAWN BY R.VELEZ
LAST REVISED BY D.FREEMAN
APPROVED BY R.BOUCHAL
DESIGN DATE 1993:04:04
LAST MODIFIED DATE 1996:02:15
SHEET 6 OF 10


SIN/COS
LOOK UP TABLE
SIN/COS
DIGITAL TO ANALOG
CONVERTER
CURRENT
TO VOLTAGE
CONVERTER
UNIPOLAR TO
BIPOLAR CONVERSION &
ELECTRONIC OFFSET ADJUST
U213
27C512
U315
7528
U415
OP_QUAD
[6] LUT.EN/
[6] LUT.WR/
NOTE: CUTTABLE TRACES
+5V
LUT.<A0:A11>
DATA
ADDRESS
uP CONTROL
STP_GAIN
LUT.A0
LUT.WR/
LUT.EN/
DGND
AGND
RFB
VREF
OUT
VDD
A/B
WR
CS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
R414
10k
C4141
220p
STEPPER
PHASE A
TP4141
A_PHASE
(+/-5V SINE)
CMA [8]
R4151
OMIT
100K
SINE_OFF
C4142
STEPPER
PHASE B
TP4142
B_PHASE
(+/-5V COSINE)
CMB [8]
R4121
COS_OFF
STEPPER GAIN ADJUST
U413
7528
U416
OP_QUAD
A4
RW
DAC0.WR/
D8
D9
D10
D11
D12
D13
D14
D15
STP_GAIN
(42)
(DAC0 address=42)
ANALOG VIEW
TP417
A_VIEW
(52)
AGND
TP617
U412
OMIT
STEPPER OFFSET ADJUST (OMIT)
DAC1.WR/
(DAC1 address=44)
NOTE: CUTTABLE TRACE
SINE_OFF
(44)
COS_OFF
(54)
[8] +5VR
SIN/COS GENERATOR
(CTP ALE BOARD)
DESIGNED BY
J.MADELEY
DOCUMENT NUMBER
10-0732C-D-SD07
LAST ECO
A237
DRAWN BY
R.VELEZ
LAST REVISED BY
D.FREEMAN
APPROVED BY
R.BOUCHAL
DESIGN DATE
1991:07:18
LAST MODIFIED DATE
1996:02:15
SHEET
7 OF 10

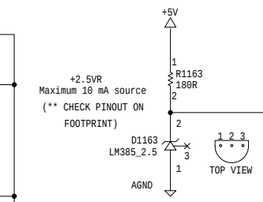

CURRENT SENSE AMP
ERROR AMP
PWM COMPARATOR
BRIDGE CONTROL
A PHASE BRIDGE AND CURRENT LIMIT
B PHASE BRIDGE AND CURRENT LIMIT
MASTER TIMING
SUPPLY MONITOR
+/-5V REFERENCE
ACS+
ACS-
BCS+
BCS-
CM.PWM [6]
CM.PWR [6]
VPWM
CMA [7]
CMB [7]
+/- 5V FS
HMIN
LMIN
CM.O_CUR [3,8,9]
CM.Q5 [6]
+12VOK [3]
CM.+12V/
+5VR [7, 8]
-5VR
TRIP POINT = 8.9V
TRIP POINT = 53.9V
CARRIAGE MOTOR
STEPPER DRIVER
(CTP ALE BOARD)
DESIGNED BY
R.B.ALLAN
DOCUMENT NUMBER
10-0732C-D-SD08
LAST ECO
A237
DRAWN BY
C.A.DUNSFORD
LAST REVISED BY
D.FREEMAN
APPROVED BY
R.BOUCHAL
DESIGN DATE
1991:08:16
LAST MODIFIED DATE
1996:02:15
SHEET
8 OF 10
NOTES:
1) RESISTORS ARE 5%, 1/4W UNLESS OTHERWISE INDICATED.
2) CAPACITORS ARE 20% UNLESS OTHERWISE INDICATED.

STATUS LEDS

NOTE LED POLARITIES!
(+ TOWARDS LENSE)

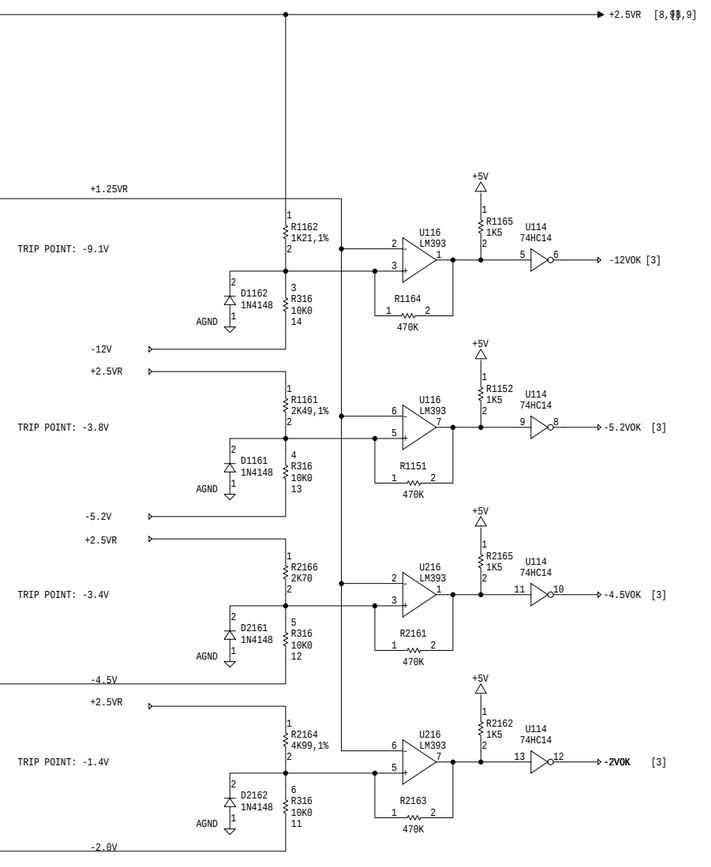


VOLTAGE REFERENCES



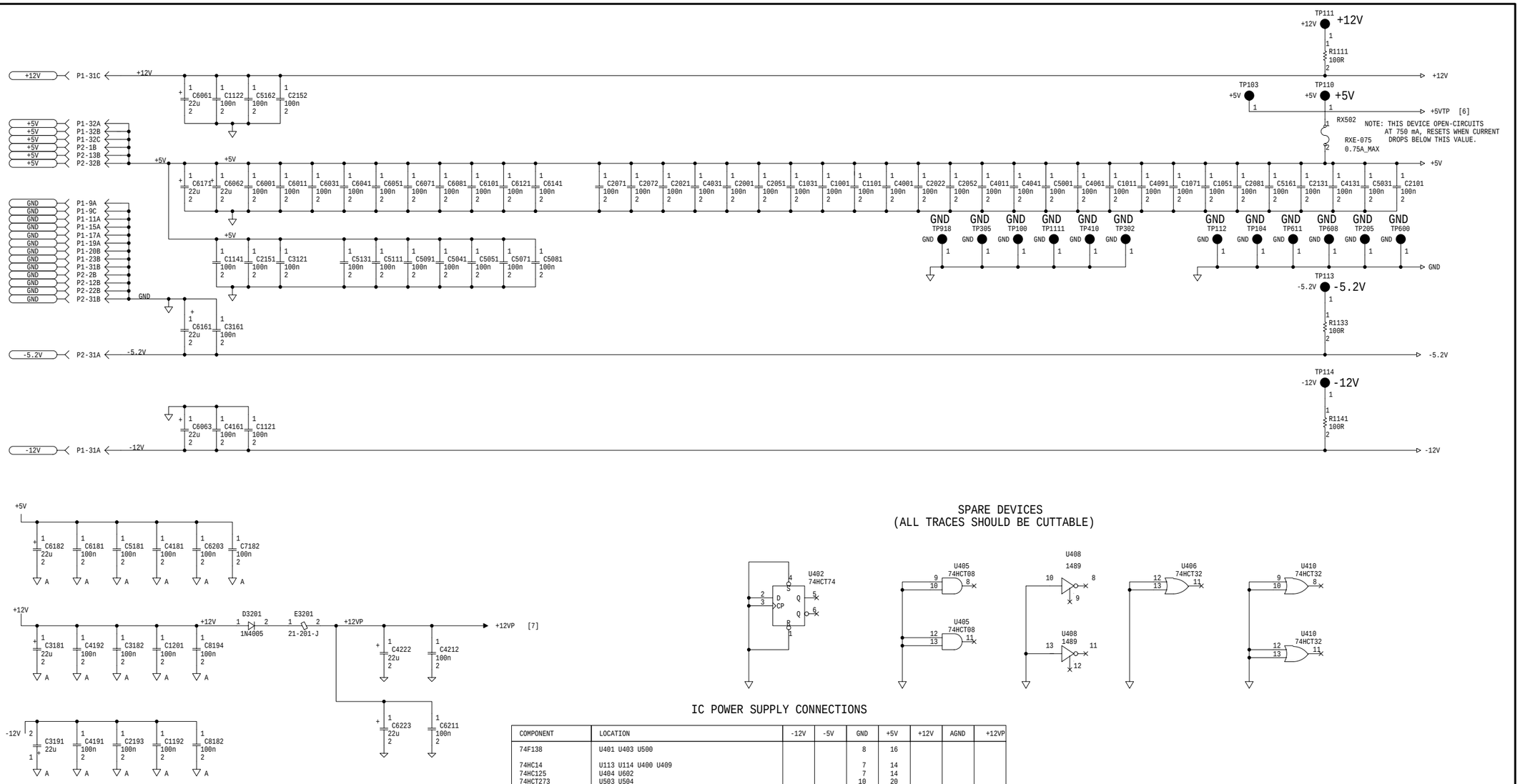
NOTE:
DS801 AND DS802 ARE QUAD PACKAGES

POWER MONITOR CIRCUITS



POWER MONITORS AND STATUS LED'S (CTP ALE BOARD)

DESIGNED BY: D.FROESE	DOCUMENT NUMBER: 10-0732C-D-SD09	LAST ECO: A237
DRAWN BY: D.FROESE	LAST REVISED BY: D.FREEMAN	APPROVED BY: R.BOUCHAL
DESIGN DATE: 1993:04:16	LAST MODIFIED DATE: 1996:02:15	SHEET: 9 OF 10



IC POWER SUPPLY CONNECTIONS

COMPONENT	LOCATION	-12V	-5V	GND	+5V	+12V	AGND	+12VP
74F138	U401 U403 U500			8	16			
74HC14	U113 U114 U400 U409			7	14			
74HC125	U404 U602			7	14			
74HCT273	U503 U504			10	20			
74HCT245	U106 U107 U505 U506 U508 U512			10	20			
74HCT245	U600 U601 U603 U604 U605 U607 U608			10	20			
74HCT08	U405			7	14			
74HCT32	U406 U410			7	14			
74HCT74	U402 U510			7	14			
74HCT541	U501			10	20			
74HCT652	U509 U511			12	24			
CY545	U208 U210			20	40			
SN75172	U609 U610 U612 U614 U615			8	16			
SN75173	U513 U514 U515 U516			8	16			
MC1488	U112	1		7		14		
MC1489	U408			7	14			
TL084	U415 U416	11				4		
OP-27	U119 U120 U818 U819	4				7		
LM319	U419	6				11		
MC34082	U219	4				8		
LM393	U116 U216 U620 U718				8		4	
PAL22V10	U418 U618				24		12	
DAC-08	U318	3				13		
TSC428	U421 U422 U621 U622			3				6
XO-54BC-8.0MHz.	U518			7	14			
XO-54BC-16.0MHz.	U312			7	14			
7528 DAC	U315 U412 U413			5	17		1	
27C512 EPROM	U213			14	28			

COMPONENT	LOCATION	GND	+5V
XC4004A	U205	1, 12, 21, 31, 43, 52, 64, 76	2, 11, 22, 33, 42, 54, 63, 74
XC4003A	U202	1, 12, 21, 31, 43, 52, 64, 76	2, 11, 22, 33, 42, 54, 63, 74

POWER SUPPLY INPUT AND SPARES (CTP ALE BOARD)

DESIGNED BY	DOCUMENT NUMBER	LAST ECO
D.FROESE	10-0732C-D-SD10	A237
DRAWN BY	LAST REVISED BY	APPROVED BY
D.FROESE	D.FREEMAN	R.BOUCHAL
DESIGN DATE	LAST MODIFIED DATE	SHEET
1993:04:16	1996:02:15	10 OF 10