## ADDRESS DECODING

DEVICE ADDRESSES:

| | | |
|---|---|---|
| VERSION REG. | (RD) | 00 - 01 |
| CBL DETECT REG. | (RD) | 02 - 03 |
| PWR STATUS REG. | (RD) | 04 - 05 |
| EXTERNAL INPUTS | (RD) | 06 - 07 |
| PM STATUS REG. | (RD) | 08 - 09 |
| PY CONTROLLER | (RD) | 0A - 0B |
| PZ CONTROLLER | (RD) | 0C - 0D |
| ALE OUTPUT REG. | (WR) | 40 - 41 |
| CM GAIN DAC | (WR) | 42 - 43 |
| CM OFFSET DAC | (WR) | 44 - 45 |
| PM CONTROL REG. | (WR) | 46 - 47 |
| PY CONTROLLER | (WR) | 48 - 49 |
| PZ CONTROLLER | (WR) | 4A - 4B |
| RESET ALE | (WR) | 4C - 4D |
| CM XILINX 0 | (R/W) | 80 - BF |
| CM XILINX 1 | (R/W) | C0 - FF |

NOTE:
MP MUST WRITE TO 0xxx4C
WITH D8 CLEARED TO BRING
ALE OUT OF RESET.

NOTE:
DATA DIRECTION IS A -> B
WHEN DIR IS HIGH.

## VERSION REGISTER

NOTE:
ADD JUMPERS
TO CHANGE VERSION
SIGNATURE

DEVICE ADDRESS = 00

DEVICE ADDRESS = 40

NOTE:
ENABLE SIGNALS INVERTED
SO SPARES ARE INACTIVE
ON RESET.

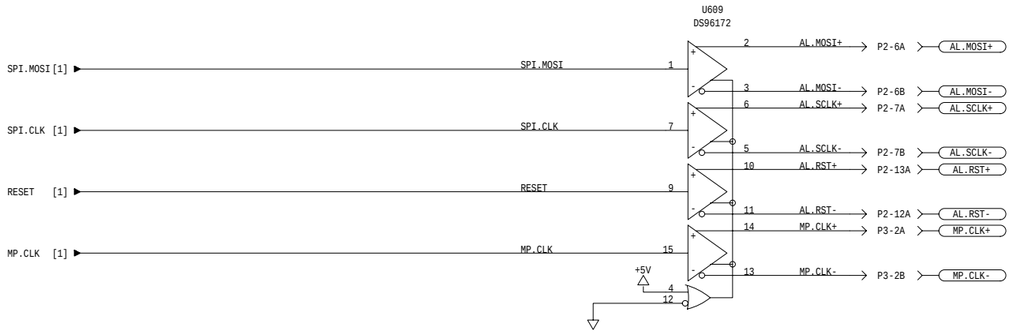
uP CONTROL BUS
uP ADDRESS BUS
uP DATA BUS
SPI ADDRESS BUS

# MASTER PROCESSOR INTERFACE (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3691A-A-SD01 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:02:12 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 1 OF 10 |

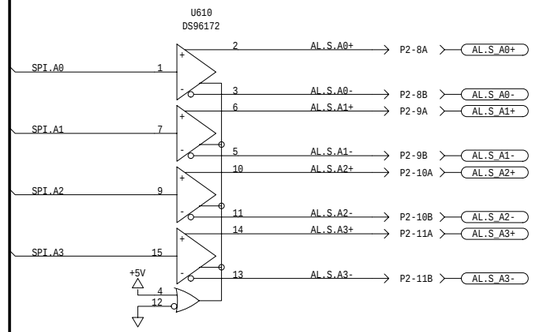
SPI ADDRESS [1]

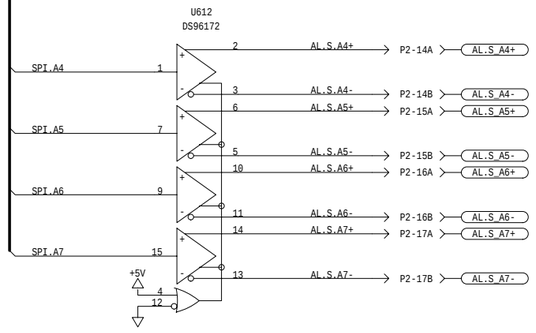
## SPI DATA AND SPARE OUTPUTS RS 485 DRIVERS




NOTE: SPI DATA INPUT SIGNAL (MISO) ON PG. 4

## SPI ADDRESS BUS RS 485 DRIVERS




CREO

# SPI BUS INTERFACE (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3691A-A-SD02 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:03:01 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 2 OF 10 |

uP DATA BUS

## ALE STATUS AND EXTERNAL INPUTS

EXT.RD/ [1]

PP.Y_HOME+ P2-21A — PP.YHOM+ — R6161 100R — R616 2K2 — U615 DS96173 pin 3
PP.Y_HOME- P2-22A — PP.YHOM-
PP.Y_AWAY+ P2-23A — PP.YAWY+ — pin 13
PP.Y_AWAY- P2-24A — PP.YAWY-
PP.Z_HOME+ P3-11C — PP.ZHOM+ — pin 5
PP.Z_HOME- P3-11B — PP.ZHOM-
PP.Z_AWAY+ P3-12C — PP.ZAWY+ — pin 11
PP.Z_AWAY- P3-12B — PP.ZAWY-
+5V — pin 4, pin 12

PP.SPR_OUT+ P3-8C — PP.SPO+ — R6221 100R — R622 2K2 — U621 DS96173 pin 3
PP.SPR_OUT- P3-8B — PP.SPO-
LU.QUEUE+ P3-13C — LU.QUE+ — pin 13
LU.QUEUE- P3-13B — LU.QUE-
LU.TE+ P3-14C — LU.TE+ — pin 5
LU.TE- P3-14B — LU.TE-
LU.LDG+ P3-17C — LU.LDG+ — pin 11
LU.LDG- P3-17B — LU.LDG-
+5V — pin 4, pin 12

R107 10K0 — +5V — 2 3 4 5 6 7 8 9 10

U107 74HCT245 — +5V — pin 19 G, pin 1 DIR

| | | | |
|---|---|---|---|
| Y.HOME | 2 | A0 B0 | 18 D0 |
| Y.AWAY | 3 | A1 B1 | 17 D1 |
| Z.HOME | 4 | A2 B2 | 16 D2 |
| Z.AWAY | 5 | A3 B3 | 15 D3 |
| PP.SPRIN | 6 | A4 B4 | 14 D4 |
| LU.QUEUE | 7 | A5 B5 | 13 D5 |
| LU.TE | 8 | A6 B6 | 12 D6 |
| LU.LDG | 9 | A7 B7 | 11 D7 |

DEVICE ADDRESS = 06

R505 10K0 — +5V — 1 — 2 3 4 5 6 7 8 9 10

U505 74HCT245 — +5V — pin 19 G, pin 1 DIR

EXT.RD/ — R406 10K0

| | | | |
|---|---|---|---|
| CM.O_CUR | 2 | A0 B0 | 18 D8 |
| PY.LIMIT | 3 | A1 B1 | 17 D9 |
| | 4 | A2 B2 | 16 D10 |
| PY.FLT | 5 | A3 B3 | 15 D11 |
| SP1.CBL/ | 4 — 13 | A4 B4 | 14 D12 |
| SP1.PWR | 5 — 12 | A5 B5 | 13 D13 |
| | 6 | A6 B6 | 12 D14 |
| | 7 | A7 B7 | 11 D15 |
| | 8 | | |
| | 9 | | |

R4061 10K0 — 5

DEVICE ADDRESS = 06

CM.O_CUR [8]
PY.LIMIT [4]
[4]
PY.FLT [4]

SP1.CBL/ P2-22C — SP1.CBL/
SP1.PWR P2-12C — SP1.PWR
CM.12OK [8]

NOTE:
THIS REGISTER WILL READ 00
IF ALL CABLES ARE PRESENT.

## CABLE DETECTS

R508 10K0 — +5V — 2 3 4 5 6 7 8 9 10

CBL.RD/ [1]

U506 74HCT245 — +5V — pin 19 G, CBL.RD/, pin 1 DIR

R507 10K0

| | | | |
|---|---|---|---|
| PP.CBL/ | P2-28A | A0 B0 | 18 D8 |
| LU.CBL/ | P3-30C | A1 B1 | 17 D9 |
| HA.CBL/ | P2-13C | A2 B2 | 16 D10 |
| CM.CBL1/ | P2-32C | A3 B3 | 15 D11 |
| PY.CBL1/ | P3-1B | A4 B4 | 14 D12 |
| PY.CBL2/ | P3-1C | A5 B5 | 13 D13 |
| CM.CBL2/ | P3-1A | A6 B6 | 12 D14 |
| | | A7 B7 | 11 D15 |

CM.CBL3 [8]

DEVICE ADDRESS = 02

TRAILING EDGE CLAMP DETECT INTERRUPT → LU.TE [6]
PLATE QUEUED INTERRUPT → LU.QUEUE [6]

ALE STATUS [5,8,9]

## POWER DETECTS

NOTE:
THIS REGISTER WILL READ FF
IF ALL POWER SUPPLIES OK.

PWR.RD/ [1]

U508 74HCT245 — +5V — pin 19 G, PWR.RD/, pin 1 DIR

R406 10K0

| | | | |
|---|---|---|---|
| PP.PWR | P2-27A | A0 B0 | 18 D8 |
| LU.PWR | P3-27C | A1 B1 | 17 D9 |
| CM.PWR | | A2 B2 | 16 D10 |
| -2VOK | | A3 B3 | 15 D11 |
| -4.5VOK | | A4 B4 | 14 D12 |
| -5.2VOK | | A5 B5 | 13 D13 |
| +12VOK | | A6 B6 | 12 D14 |
| -12VOK | | A7 B7 | 11 D15 |

10K0 R4061 — 2 3 10 — 1

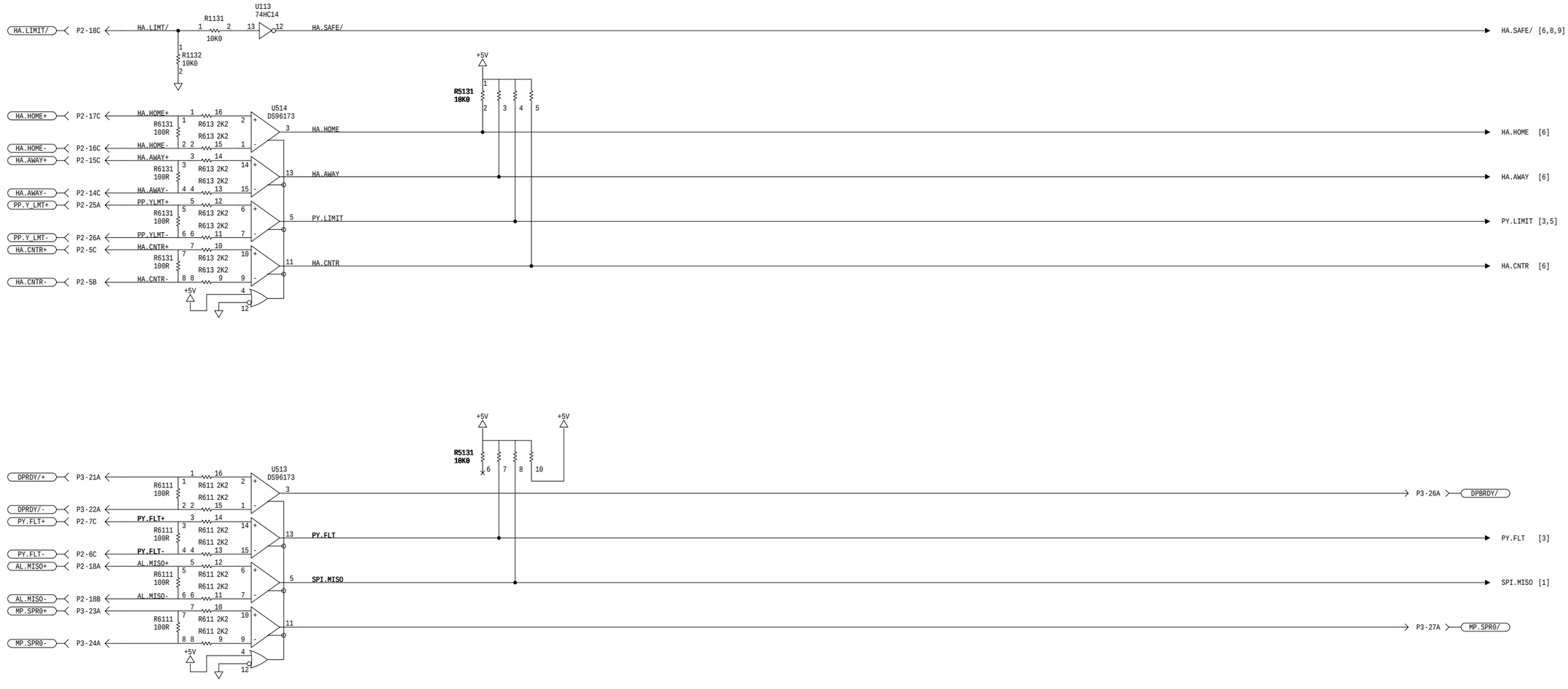
DEVICE ADDRESS = 04

CM.PWR [8]
-2VOK [9]
-4.5VOK [9]
-5.2VOK [9]
+12VOK [9]
-12VOK [9]

CREO

# INPUT REGISTERS (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3691A-A-SD03 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:02:12 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 3 OF 10 |




CREO

# HOME / AWAY BOARD INTERFACE (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3961A-A-SD04 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:02:12 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 4 OF 10 |

PICK.RD/ [1]
SP1.OUT1 [1]
PY.LIMIT [4]

## PICKER CONTROL REGISTER

U504 74HCT273
RESET/ [1]
PICK.WR/ [1]
DATA BUS [1]
RESET [1]
D8 D9 D10 D11 D12 D13 D14 D15
PY.RESET PY.REQ PY.ABORT PZ.RESET PZ.REQ QUEUE.EN PZ.ABORT
DEVICE ADDRESS = 46

Y.AWAY [3]
Y.HOME [3]
U113 74HC14

PY.WR/ [1]
PY.RD/ [1]
U510 74HCT74

## Y-AXIS I/O REGISTER

U511 74HCT652
PY.BUSY/
PY.DATA/
U410 74HCT32
U113 74HC14
READ ADDRESS = 0A
WRITE ADDRESS = 48
R2101 10K0

U410 74HCT32
RESET PY.RESET
PY.ABORT
PY.REQ
U312 16MHz. CMOS CRYSTAL OSC.

PY.RXD [5]
U210 CY545
PY.RXD PY.RST PY.AWAY/ PY.HOME/ PY.ABRT/ 16MHZCLK PY.REQ/
PICY_D0 PICY_D1 PICY_D2 PICY_D3 PICY_D4 PICY_D5 PICY_D6 PICY_D7
PULSE/ CCW STOPPED SLEW/ MEM_SEL/ HP_SEL/ SW_SEL/ WR/ RD/ ALE TXD FPL/ BUSY/ RESERVED USRB0 USRB1 USRB2 USRB3 USRB4 USRB5
PY.PULSE PY.DIR PY.STOP PY.TXD PY.DATA/ PY.BUSY/ PY.HOME/
R2102 10K0

U409 74HC14
PY.LIMIT
U405 74HCT08
PY.LIMT/ PY.PULSE

U614 DS9617
PY.PLS PY.DIR PY.STOP SP1.OUT1
PY.YPULSE+ PY.YPLS- PY.YDIR+ PY.YDIR- PY.YSTP+ PY.YSTP-
P2-19C P2-19B P2-20C P2-20B P2-21C P2-21B
PY.YPULSE+ PY.YPULSE- PY.YDIR+ PY.YDIR- PY.YSTOP+ PY.YSTOP-

## PICKER STATUS REGISTER

U512 74HCT245
PICK.RD/
PY.STOP PY.DIR PY.DATA/ PY.BUSY/ PZ.STOP PZ.DIR PZ.DATA/ PZ.BUSY/
DEVICE ADDRESS = 08
DATA BUS [1]

## RS-232 INTERFACE

NOTE: INSTALL THESE PARTS FOR DEVELOPMENT ONLY
J2121 U408 1489 PY.RXD
U112 1488 PY.TXD PZ.TXD
J2122 U408 1489 PZ.RXD

## PICKER Y-AXIS STEPPER CONTROLLER

## PICKER Z-AXIS STEPPER CONTROLLER

Z.HOME [3]
Z.AWAY [3]
LU.QUEUE [3]
U409 74HC14
U405 74HCT08 QUEUE.EN LU.QUEUE
U406 74HCT32 PZ.RESET PZ.QUE PZ.ABORT
PZ.REQ

PZ.RXD [5]
U208 CY545
PZ.RXD PZ.RST PZ.AWAY/ PZ.HOME/ PZ.ABRT/ 16MHZCLK PZ.REQ/
PICKZ_D0 PICKZ_D1 PICKZ_D2 PICKZ_D3 PICKZ_D4 PICKZ_D5 PICKZ_D6 PICKZ_D7
PZ.PULSE PZ.DIR PZ.STOP PZ.TXD PZ.DATA/ PZ.BUSY/ PZ.HOME/
R2082 10K0

U620 DS9617
PZ.PULSE PZ.DIR PZ.STOP PY.ENBL
PP.ZPLS+ PP.ZPLS- PP.ZDIR+ PP.ZDIR- PP.ZSTP+ PP.ZSTP- PY.ENBL+ PY.ENBL-
P3-3C P3-3B P3-4C P3-4B P3-7C P3-7B P2-11C P2-10C
PP.ZPULSE+ PP.ZPULSE- PP.ZDIR+ PP.ZDIR- PP.ZSTOP+ PP.ZSTOP- PY.ENBL+ PY.ENBL-

## Z-AXIS I/O REGISTER

PZ.WR/ [1]
PZ.RD/ [1]
U510 74HCT74
U509 74HCT652
PZ.BUSY/ PZ.DATA/
U406 74HCT32
U409 74HC14
R2081 10K0
READ ADDRESS = 0C
WRITE ADDRESS = 4A

DATA BUS [1]
PY.ENBL [1]

CREO

# PICKER STEPPER CONTROLLER (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3691A-A-SD05 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993;03:29 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 5 OF 10 |

NOTE:
THIS HEADER IS FOR DOWNLOADING LCA CONFIGURATION FILES INSTALL ON DEVELOPMENT BOARDS ONLY.

[10] +5VTP
XCHECK.1 J501-1 +5VTP
XCHECK.2 J501-2 GND
XCHECK.4 J501-4 CCLK
XCHECK.5 J501-5 DONE
XCHECK.6 J501-6 D8
XCHECK.7 J501-7 PROGRAM/
XCHECK.8 J501-8 INIT/
XCHECK.9 J501-9
[8] INIT/
[8] DONE
[1] PROG.AL/
LCA.PRG/ P1-14B
U602 74HC125
PROGRAM/

READBACK HEADER
RT.1 J106-1 M0.1
RD.1 J106-2 M1.1
TRIG.1 J106-3 RS.1/

READBACK HEADER
RT.2 J103-1 M0.2
RD.2 J103-2 M1.2
TRIG.2 J103-3 RS.2/

R501 10K
R602 10K
R202 10K
R404 10K
+5V

U501 74HCT541
PROG.AL/ G1
DONE G2
SEL.AL/
MP.CLK/
RW
U400 74HC14

U205 XC4005E-4PC84C
M0 M1 M2 CS0 CS1 WS RS PROGRAM
RDY INIT DONE CCLK DOUT TDO
XSPR0 LUT.A11
CLOCK RW CS
A1 A2 A3 A4 A5 RESET
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
D8 (DIN) INT
(HDC) LUT.EN LUT.WR LUT.A0 LUT.A1 LUT.A2 LUT.A3 LUT.A4 LUT.A5 LUT.A6 LUT.A7 LUT.A8 LUT.A9 LUT.A10
SCLK8 DEADSCAN RUN HOME AWAY SAFE TE_CLAMP LU_QUEUE
EQ INCR_DIR INCR RST_POS (LDC)PLT_EQ
ADDRESS = 80 - BF

U202 XC4005E-4PC84C
M0 M1 M2 CS0 CS1 WS RS PROGRAM DIN
RDY INIT DONE CCLK DOUT TDO HDC LDC
XSPR0 CENTRE
CLOCK RW CS
A1 A2 A3 A4 A5 RESET
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
SCLK8
INCR_DIR INCR RST_POS PLT_EQ DEADSCAN RUN NEWLINE
SPARE0 SPARE1 SPARE2 SPARE3 SPARE4 SPARE5 SPARE6 SPARE7 SPARE8
EQ
HA.CNTR
AL_SPR0 AL_SPR1 CM_Q5 CM_PWM
ADDRESS = C0 - FF

NOTE:
XILINX OUTPUTS ARE TTL LEVELS

NOTE:
D8 -> D15 MUST BE CONNECTED TO LCA.D0 -> D7 FOR CONFIGURATION DOWNLOAD

NOTE:
UNUSED PINS = 5, 17, 19, 20, 62, 70, 83

RDY P1-13B LCA.RDY
INIT/ P1-13C LCA.INIT/
DONE P1-14A LCA.DONE
U602 74HC125

DONE [9]
DIR [8]
PULSE [8]
PROGRAM/ [8]
SH.DATA [8]

[1] SCLK8
[1] DEADSCN/
[1] RUN/
[4] HA.HOME
[4] HA.AWAY
[4] HA.SAFE/
[3] LU.TE
[3] LU.QUEUE
[1] MP.SPR0
[1] MP.SPR1
[1] MP.SPR2
[1] DP.SPR0
[1] DP.SPR1
[1] NEWLINE/
[4] HA.CNTR
[8] CM.PWM
[8] CM.Q5

AL.SPR0 [1]
AL.SPR1 [1]

LUT<A0:A11>
[7]

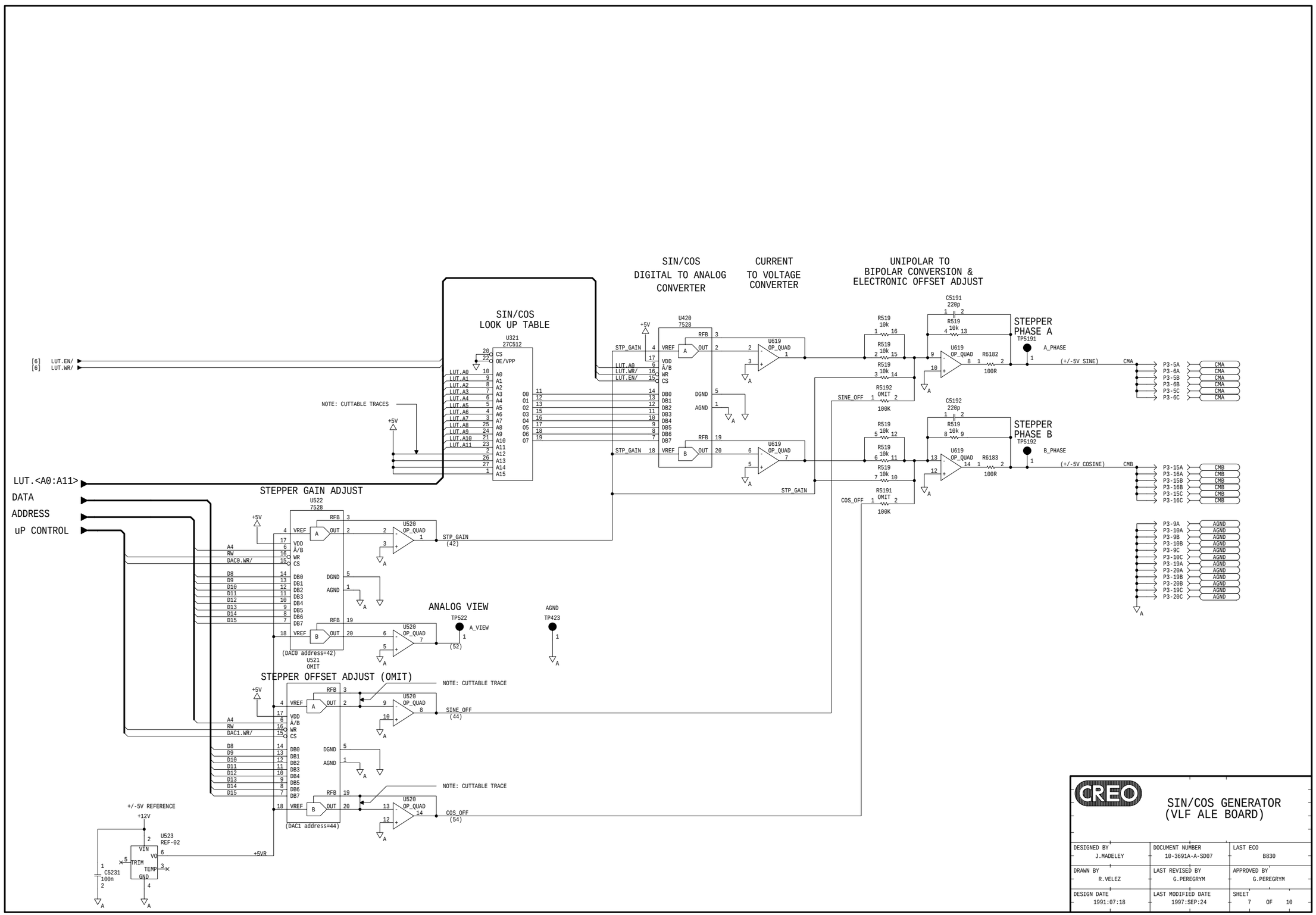
INT/ [1]
LUT.EN/ [7]
LUT.WR/ [7]

uP CONTROL
ADDRESS
DATA

CREO

# CARRIAGE SYNTHESIZER (VLF ALE BOARD)

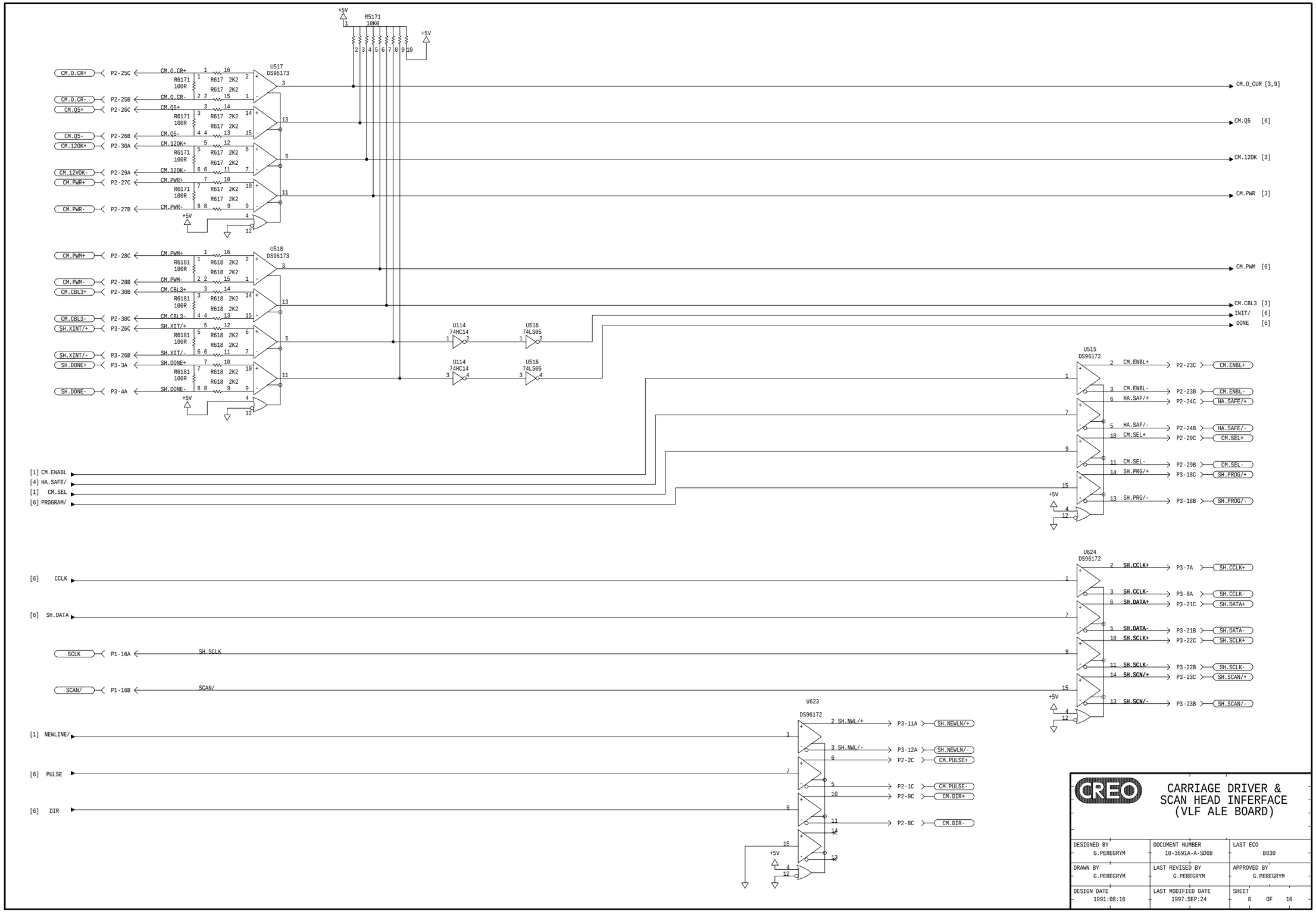
| | | |
|---|---|---|
| DESIGNED BY: R.VELEZ | DOCUMENT NUMBER: 10-3691A-A-SD06 | LAST ECO: B830 |
| DRAWN BY: R.VELEZ | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:04:04 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 6 OF 10 |




CREO

# SIN/COS GENERATOR (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY: J.MADELEY | DOCUMENT NUMBER: 10-3691A-A-SD07 | LAST ECO: B830 |
| DRAWN BY: R.VELEZ | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1991:07:18 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 7 OF 10 |




CREO

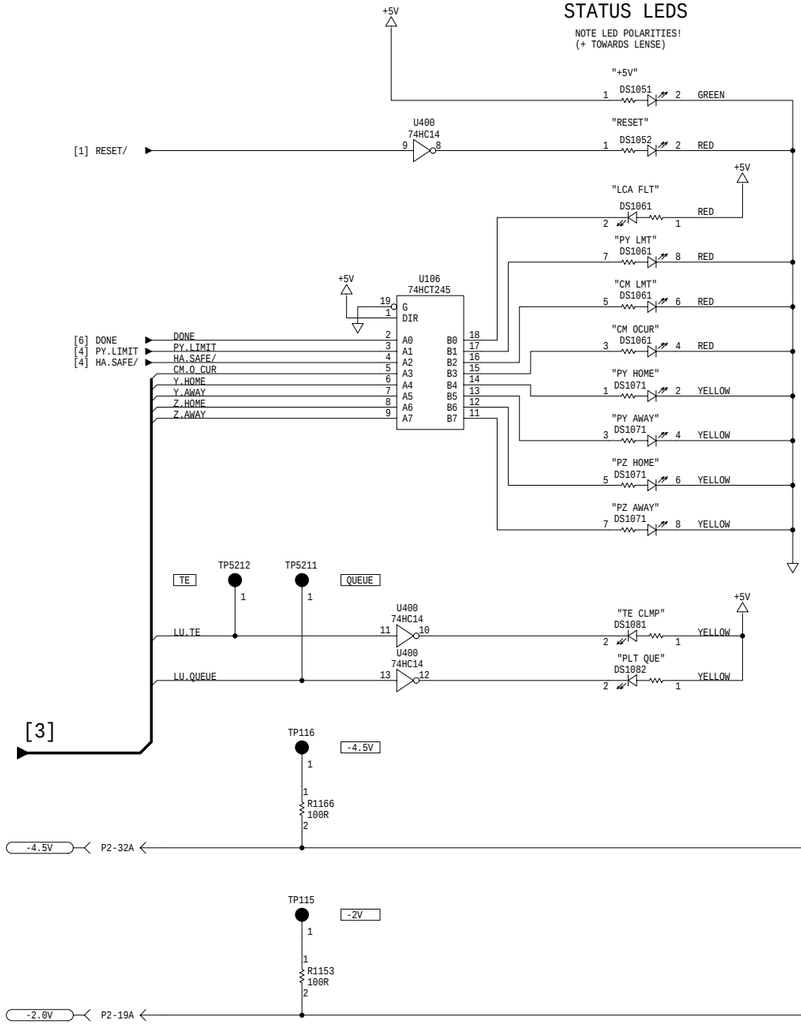
# CARRIAGE DRIVER & SCAN HEAD INFERFACE (VLF ALE BOARD)

| | | |
|---|---|---|
| DESIGNED BY G.PEREGRYM | DOCUMENT NUMBER 10-3691A-A-SD08 | LAST ECO B830 |
| DRAWN BY G.PEREGRYM | LAST REVISED BY G.PEREGRYM | APPROVED BY G.PEREGRYM |
| DESIGN DATE 1991:08:16 | LAST MODIFIED DATE 1997:SEP:24 | SHEET 8 OF 10 |

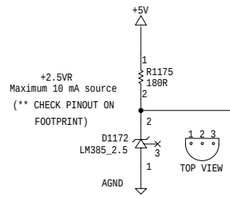
# POWER MONITOR CIRCUITS

## STATUS LEDS

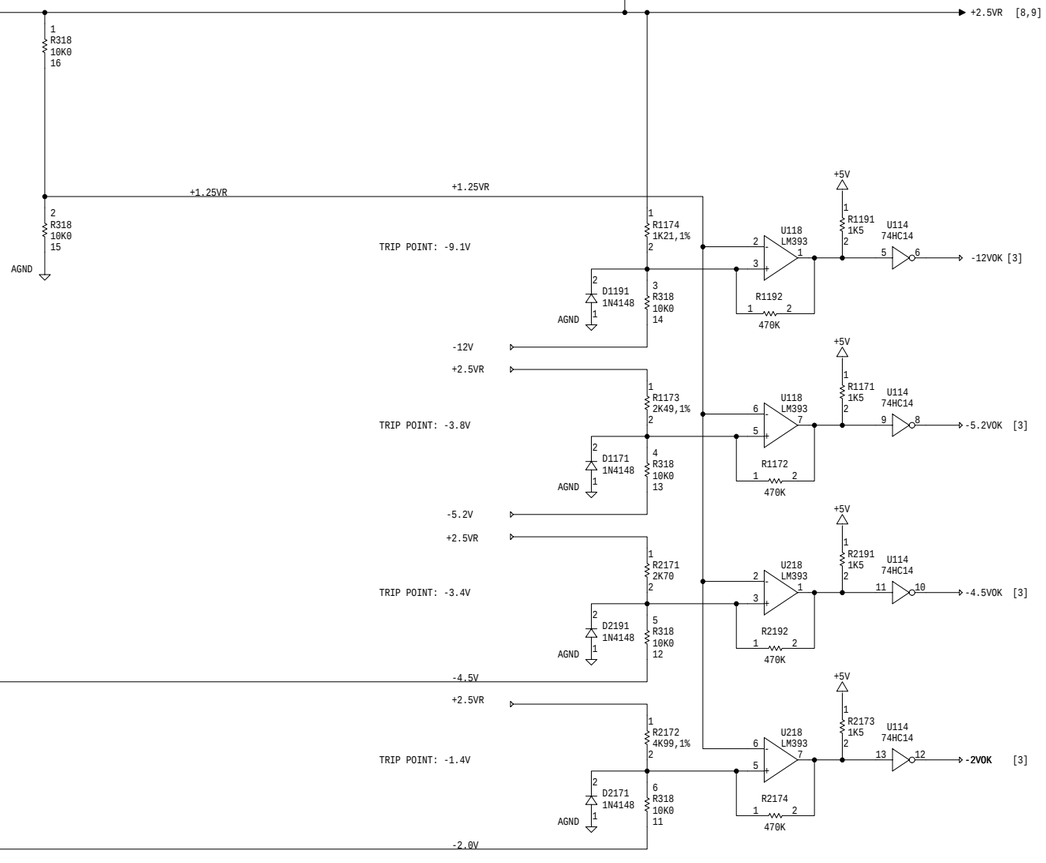
NOTE LED POLARITIES!
(+ TOWARDS LENSE)



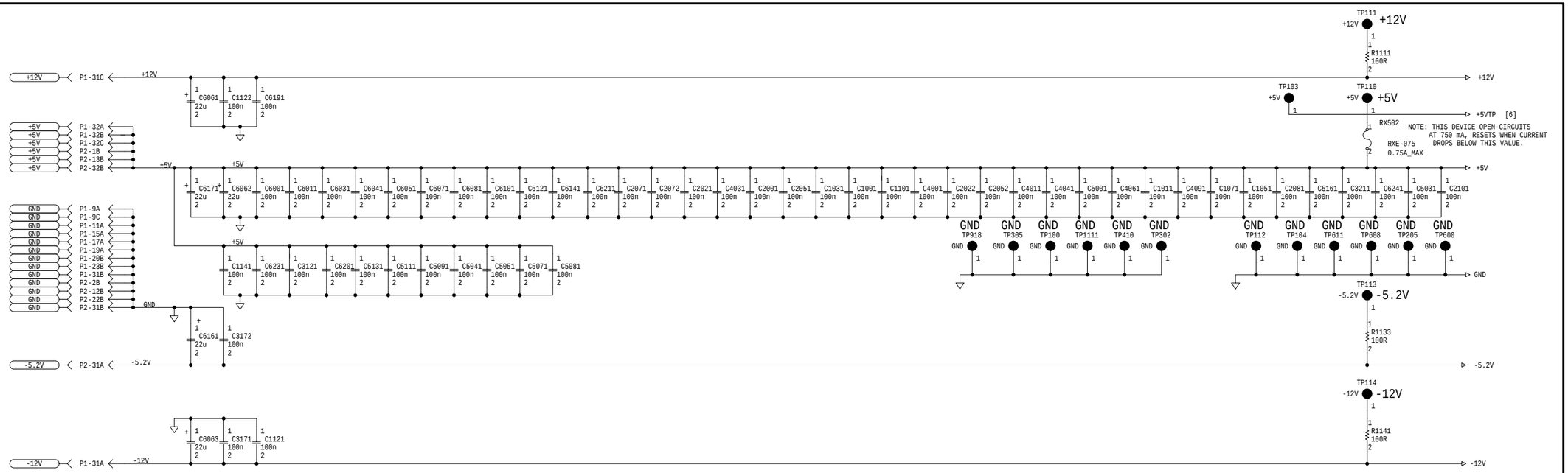

## VOLTAGE REFERENCES

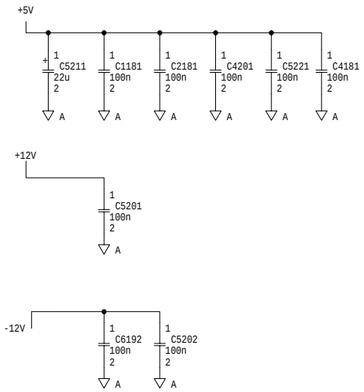



NOTE:
DS801 AND DS802 ARE QUAD PACKAGES

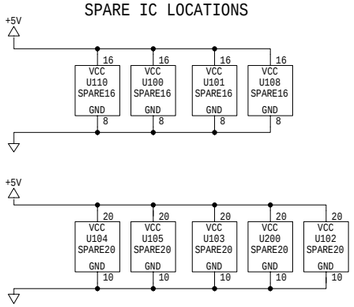



| | | |
|---|---|---|
| POWER MONITORS AND STATUS LED'S (VLF ALE BOARD) | | |
| DESIGNED BY: D.FROESE | DOCUMENT NUMBER: 10-3691-A-SD09 | LAST ECO: B830 |
| DRAWN BY: D.FROESE | LAST REVISED BY: G.PEREGRYM | APPROVED BY: G.PEREGRYM |
| DESIGN DATE: 1993:04:16 | LAST MODIFIED DATE: 1997:SEP:24 | SHEET: 9 OF 10 |

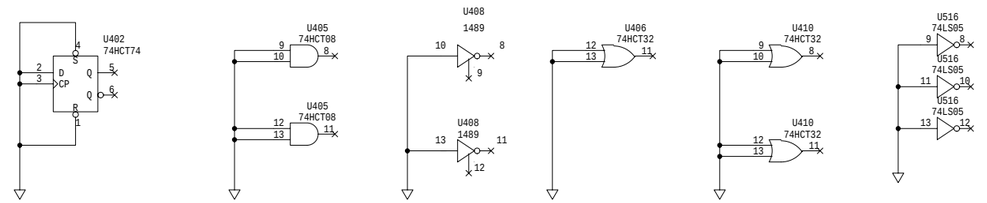



## SPARE IC LOCATIONS




## SPARE DEVICES
## (ALL TRACES SHOULD BE CUTTABLE)




## IC POWER SUPPLY CONNECTIONS

| COMPONENT | LOCATION | -12V | -5V | GND | +5V | +12V | AGND | +12VP |
|---|---|---|---|---|---|---|---|---|
| 74F138 | U401 U403 U500 | | | 8 | 16 | | | |
| 74HC14 | U113 U114 U400 U409 | | | 7 | 14 | | | |
| 74HC125 | U404 U602 | | | 7 | 14 | | | |
| 74HCT273 | U503 U504 | | | 10 | 20 | | | |
| 74HCT245 | U106 U107 U505 U506 U508 U512 | | | 10 | 20 | | | |
| 74HCT245 | U600 U601 U603 U604 U605 U607 U608 | | | 10 | 20 | | | |
| 74HCT00 | U405 | | | 7 | 14 | | | |
| 74HCT32 | U406 U410 | | | 7 | 14 | | | |
| 74HCT74 | U402 U510 | | | 7 | 14 | | | |
| 74HCT541 | U501 | | | 10 | 20 | | | |
| 74HCT652 | U509 U511 | | | 12 | 24 | | | |
| CY545 | U208 U210 | | | 20 | 40 | | | |
| SN75172 | U609 U610 U612 U614 U615 | | | 8 | 16 | | | |
| SN75173 | U513 U514 U515 U516 | | | 8 | 16 | | | |
| MC1488 | U112 | 1 | | 7 | | 14 | | |
| MC1489 | U408 | | | 7 | 14 | | | |
| TL084 | U415 U416 | 11 | | | | 4 | | |
| OP-27 | U119 U120 U818 U819 | 4 | | | | 7 | | |
| LM319 | U419 | 6 | | | | 11 | | |
| MC34082 | U219 | 4 | | | | 8 | | |
| LM393 | U116 U216 U620 U718 | | | | 8 | | 4 | |
| PAL22V10 | U418 U618 | | | | 24 | | 12 | |
| DAC-08 | U318 | 3 | | | | 13 | | |
| TSC428 | U421 U422 U621 U622 | | | 3 | | | | 6 |
| XO-54BC-8.0MHz. | U518 | | | 7 | 14 | | | |
| XO-54BC-16.0MHz. | U312 | | | 7 | 14 | | | |
| 7528 DAC | U315 U412 U413 | | | 5 | 17 | | 1 | |
| 27C512 EPROM | U213 | | | 14 | 28 | | | |

| COMPONENT | LOCATION | GND | +5V |
|---|---|---|---|
| XC4005E | U202,U205 | 1, 12, 21, 31, 43, 52, 64, 76 | 2, 11, 22, 33, 42, 54, 63, 74 |

CREO

# POWER SUPPLY INPUT AND SPARES (VLF ALE BOARD)

| DESIGNED BY | DOCUMENT NUMBER | LAST ECO |
|---|---|---|
| D.FROESE | 10-3691A-A-SD10 | B830 |
| DRAWN BY | LAST REVISED BY | APPROVED BY |
| D.FROESE | G.PEREGRYM | G.PEREGRYM |
| DESIGN DATE | LAST MODIFIED DATE | SHEET |
| 1993:04:16 | 1997:SEP:24 | 10 OF 10 |