CreoScitex

MCE POST Release Notes

Revision History

Revision	Date	Author	Comments
1.06	21-Aug-2003	Peter Bai	Release Notes for V1.06
1.05	10-Dec-2001	Lane Wilson	Release Notes for V1.05
1.04	13-Sep-2001	Lane Wilson	Release Notes for V1.04

CONTENTS

Revision History 1

1. Introduction 1
   - 1.1 Operation 1
     - 1.1.1 Power On Condition 1
     - 1.1.2 Firmware Reset Condition 1
     - 1.1.3 Visual Status Indication 1
     - 1.1.4 Aborting the Tests 1
     - 1.1.5 Staying in POST Code 1
     - 1.1.6 Accessing Post code from Main code 1
   - 1.2 Operation 2
   - Changes from Previous v1.05 of POST 2
   - Changes from Previous v1.04 of POST 2
   - Changes from Previous v1.03 of POST 2

2. POST Commands 4
   - 2.1 Tests 4
     - 2.1.1 Test 9010 – 1M SRAM 4
     - 2.1.2 Test 9011 – 32K Non-Volatile SRAM 5
     - 2.1.3 Test 9012 – 16C554 Quad Uart Test 5
     - 2.1.4 Test 9013 – 68376 SCI Uart Test 6
     - 2.1.5 Test 9014 – NVS Sram Verification 6
     - 2.1.6 Test 9015 – NVS Flash Verification 6
   - 2.2 Enable NNNN 6
   - 2.3 Disable NNNN 6

2.4 Reset.....7

1. INTRODUCTION

This document provides information on the MCE POST code module. The POST code provides the *Power-On-Self-Test* functionality for the MCE board. This code module is not specific to any product that uses an MCE board.

1.1 Operation

1.1.1 Power On Condition

When the MCE board is powered on, or the reset button is pushed, the POST code will execute all of the power on tests. This takes less than a minute.

1.1.2 Firmware Reset Condition

If the "reset xxxx" command is executed from the mce board's firmware (boot, post, or main) then the POST code will not execute the normal power on self tests. All it will do is verify the integrity of the main firmware, and start it running.

1.1.3 Visual Status Indication

While the POST code is running, both of the green status Leds, Idle and Heartbeat will flash on and off together at a rate of 750msec.

1.1.4 Aborting the Tests

If during power up POST testing, you do not wish to wait for the tests to complete, you can send the ascii <CR> character to abort the tests. This will typically be the 'Enter' key on most terminal programs.

1.1.5 Staying in POST Code

To stay in the POST code while it is running power up tests, first abort the tests with the 'Enter' key, and then press either the ESC or '.' (dot) key to abort the entire boot up sequence and stay in post code.

1.1.6 Accessing Post code from Main code

To access the POST code's monitor prompt, use the main firmware's command: "post reset". On some versions of main MCE firmware, you may have to enter the command: 'access dev' first, to allow the 'post reset' command to operate. Once the 'post reset' command has been accepted, it will enter the POST code in about 3-4 seconds.

1.2 Operation

This section lists history of changes for each release of MCE Post firmware.

Changes from Previous v1.05 of POST

1.Version 1.06 of the MCE Post uses the FWD subsystem for firmware directory support.

2.Version 1.06 of the MCE Post fixes the syntax errors where POST_TEST_DESCRIPTOR structures are declared.

3.The data segment of MCE Post v1.06 is moved to MCE external RAM to save more 376 CPU's internal memory for the stack and heap. The heap size is increased to 3 K while stack size is increased to 4608 bytes.

4.The MCE Post v1.06 **must** be built against the ClearCase baseline #2848.

5.The operating address of the MCE Post v1.06 has been changed to yield more flash memory space for the main firmware. Therefore, this version of MCE Post **must** be downloaded by the MCE Boot v1.12 or main firmware with FWD support.

Changes from Previous v1.04 of POST

Version 1.05 of the MCE Post code fixes a bug where sometimes the post code would crash when a "warm" reset was occurring on the MCE board. This only occurred on some MCE boards.

Changes from Previous v1.03 of POST

The following table indicates the differences between v1.04 of the MCE POST code, and the previous version of 1.03. Version 1.03 was essentially a non-functional engineering version of POST. Its SRAM memory test did not actually test memory.

Description:	V1.04	V1.03
Status LEDs	Both Heartbeat and the Idle led blink together at the 750msec on/off rate	Only the Heartbeat led blinks at 750msec on/off.
Power-On Tests Performed	1M SRAM (non-destructive) 32k BB SRAM (non-destructive) 16C554 Uart loop-back (internal) 68376 Uart loop-back (internal) Flash NVS Validity check BBRam NVS validity check	None (SRAM memory test was non-functional)
Aborting Memory Tests	Can be aborted via the 'Enter' key	n/a
Interactive Tests Provided	External loop-back connector uart tests. Can test all 5 serial ports.	None
Warm/Cold Start Detection	Only runs POST tests on powerup	N/a
Board Reset Boot Cycles	Counts each board reset cycle in battery backed NVS	None

Test Progress Indicators	Uses dots, and some letters	None
Fatal Exception Handler	Improved, now uses the 16C554 uart 'B' channel. (Diagnostic port – J38)	Uses old diagnostic port – J40

2. POST COMMANDS

Not all of the possible POST monitor commands are documented here. Only the commands associated with executing POST tests are documented.

2.1 Tests

The following test commands are to be executed by the post command: “test nnnn Y”, where ‘nnnn’ is the specific test number, and ‘Y’ is the type of test to perform. Just typing “test nnnn” implies a zero (0) type of test, which is reserved for the power-on type of test. Certain tests (9012, and 9013) have an interactive mode where must install some sort of loop-back connector first, or when directed to.

Just typing “test 99” will execute all of the power up tests.

```
Post>> test 99
9010: 1M SRAM Test ..............................PASSED
9011: 32K NonVolatile SRAM Test .................PASSED
9012: Quad Uart Test A+B+C+D+....................PASSED
9013: 68376 Uart Test A..........................PASSED
9014: NVS SRAM Verification .....................PASSED
9015: NVS Flash Verification ....................PASSED
```

Just typing ‘test’, will display a list of all available tests:

```
Post>> test
Available tests (* = factory default, + = enabled):
*   9010: 1M SRAM Test (FATAL)
*   9011: 32K NonVolatile SRAM Test (FATAL)
*   9012: Quad Uart Test
*   9013: 68376 Uart Test
*   9014: NVS SRAM Verification
*   9015: NVS Flash Verification
```

2.1.1 Test 9010 – 1M SRAM

Test the 1M of SRAM. The test consists of the following memory test primitives, all using a 16-bit word:

1. save the original memory word
2. write a 0x0000, and verify it
3. write a 0xffff and verify it
4. write (16) walking bit tests; 1-2-4-8-16---->0x8000. Verify each step
5. write lower 16 bit of memory address into memory word and verify it
6. restore the original memory word, and verify it.
7. repeat steps 1-6 for every 16-bit word in the 1M SRAM.

Progress indicators are ascii dots (.) which are displayed for every 16k memory words. A pass or fail indication is given at the end of the test. The diagnostic serial port is checked for the ascii <CR> or ‘Enter’ character while the test is running. This key will abort the test. If POST is running in a power up condition, this will abort all of the power up tests.

```
Post>> test 9010
9010: 1M SRAM Test ..............................PASSED
```

2.1.2 Test 9011 – 32K Non-Volatile SRAM

Test the 32K of Battery-Backed SRAM. The test consists of the following memory test primitives, all using an 8-bit byte:

1. save the original memory byte
2. write a 0x00, and verify it
3. write a 0xff and verify it
4. write (8) walking bit tests; 1-2-4-8-16---->0x80. Verify each step
5. write lower 8 bits of memory address into memory word and verify it
6. restore the original memory byte, and verify it.
7. repeat steps 1-6 for every 8-bit byte in the 32K SRAM.

Progress indicators are ascii dots (.) which are displayed for every 2k memory words. A pass or fail indication is given at the end of the test. The diagnostic serial port is checked for the ascii <CR> or 'Enter' character while the test is running. This key will abort the test. If POST is running in a power up condition, this will abort all of the power up tests.

```
Post>> test 9011
9011: 32K NonVolatile SRAM Test ..................PASSED
```

2.1.3 Test 9012 – 16C554 Quad Uart Test

This tests the 16C554 quad uart chip. The test consists of setting a serial channel to 57600 baud, and sending 256 binary values, 0x00 – 0xff. Each sent binary data byte is verified as being recived correctly. When run in a power up condition, each serial port is placed into an internal loop-back mode so no external loop-back test plug is required.

```
Post>> test 9012
9012: Quad Uart Test A+B+C+D+.....................PASSED
```

The progress indicators are a combination of upper case letters and dots. Letters A,B,C & D indicate which quad uart channel is being testes. A '+' character after the channel letter indicates this channel has passed, while a '-' character after the channel letter indicates the channel has failed.

Use the POST monitor command "test 9012 1" to perform an external loop-back test. You will be prompted to enter a single character: A,B,C,D, or E. Selecting A through D will select one of the 16C554 quad uart channels to test. For channels A, C, and D, ensure you have the test plug installed on connectors J37, J2, and J39. For channel B, the test will instruct you to remove the diagnostic serial cable and install the test plug on connector J38. You then need to wait until the red Service led is lit. This tells you to remove the test plug on connector J38, and replace the diagnostic serial cable. Pass or Fail indication will be given at the end of the test.

Here is an example of the test running on channel 'A':

```
Post>> test 9012 1
9012: Quad Uart Test
Serial Ports:
A=J37-DNGL_COMM B=J38-DIAG_COMM C=J2-EH_CNTL D=J
Enter which serial port to test A,B,C,D,E ? a
Testing Serial Port J37-DNGL_COMM ..........
Serial Port test has PASSED
```

Here is an example of running the test of the diagnostic port, channel ‘B’:

```
Post>> test 9012 1
9012: Quad Uart Test
Serial Ports:
A=J37-DNGL_COMM B=J38-DIAG_COMM C=J2-EH_CNTL D=J39-WS_COMM E=J40-SPR_COMM
Enter which serial port to test A,B,C,D,E ? b
Install Loopback connector on serial port J38-DIAG_COMM connector.
The test will start in 10 seconds
Remove Loopback connector when the Red Service LED is activated. PASSED
Post>>
```

2.1.4 Test 9013 – 68376 SCI Uart Test

This is the same test as the 16C554 quad uart test, but operates on the internal 68376 SCI serial port. This port uses connector J40.

An example running the power on test:

```
Post>> test 9013
9013: 68376 Uart Test A.........................PASSED
```

An example running the interactive external loop-back test:

```
Post>> test 9013 1
9013: 68376 Uart Test Testing Serial Port J40-SPR_COMM ..........PASSED
```

2.1.5 Test 9014 – NVS Sram Verification

This test will examine the contents of the battery backed 32k SRAM chip, and verify its integrity. This chip is used to hold NVS parameters, and has duplicate redundancy and error detection schemes in its stored data.

```
Post>> test 9014
9014: NVS SRAM Verification .....................PASSED
```

2.1.6 Test 9015 – NVS Flash Verification

This test will examine the contents of the two on-board flash sectors reserved for flash NVS, and verify it’s integrity. This memory is used to hold flash NVS parameters, and has duplicate redundancy and error detection schemes in its stored data.

```
Post>> test 9015
9015: NVS Flash Verification ....................PASSED
```

2.2 Enable NNNN

The monitor command ‘enable nnnn” will enable a specific POST test to run at power up time. This is normally only required if the test was previously disabled with the ‘disable nnnn’ command.

2.3 Disable NNNN

The monitor command ‘disable nnnn’ will disable a specific POST test to be bypassed at power up time. Use the monitor command ‘enable nnnn’ to re-enable it later.

2.4 Reset

The ‘reset’ monitor command will reset the MCE board and go through a complete re-boot cycle, attempting to execute BBR, BOOT, POST, and MAIN firmware.

The ‘reset boot’ monitor command will reset the MCE board and just execute the BOOT code.