

MCE LCA/FPGA/XILINX RELEASE NOTES

Release Version 2.23

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Revision History

Revision	Date	Author	Comments
2.23	Nov 3, 2004	Greg Hall	Updated with release information for 2.23
2.11	July 16, 2004	Gary Theobald	Updated with release information for 2.11
1.94	May 12, 2004	Gary Theobald	Updated with release information for 1.94 and added specific information on downloads and history

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MCE LCA/FPGA/Xilinx Release Notes
Release Version 2.23

1. 2.23 UPDATES

1.1 VERSION INFORMATION

Version 02.23 September, 2004 (GHall)
Part Number: 636-00093A

1.2 CHANGES

- Increased TSP registers scanline_count and scanline_progress to 24 bits
- Added fix to dp_ext_gate_select to fix slave-master issue in Hydra. Slave can now be designated as a slave and plot in master-slave mode as well as slave-only mode.
- Made TSP clock detection circuit less sensitive to frequency fluctations. Should help resolve "Data Channel Not Detected" errors.

1.3 FW COMPATABILITY

Compatible with:
Lotem Quantum with crg 1.44
TSM 4/8 with crg 1.44
TSM News with crg 1.44
Magnus VLF main fw 1.04 or better

2. UPGRADE PROCEDURE

To upgrade the MCE firmware, please perform the following steps:

1. This step must be performed before upgrading the firmware:

Important!

You must upgrade ServiceShell before upgrading firmware.
Use the new FirmwareUpgrade script to upgrade all the firmware.

Service Shell should always be upgraded before upgrading firmware. However, it is particularly important to upgrade to Service Shell 2.5 for this firmware version because the new upgrade script includes a special procedure that is required for properly installing the new versions of firmware.

It is critical that the new BOOT module be downloaded *before* any other new firmware module, including main firmware, POST, Xilinx, etc. For example, if you download new main firmware onto an

MCE with BOOT v1.09, the new main firmware will fail to run. To recover from this, you will have to download the previous version of whatever module(s) you have downloaded and then proceed by downloading the new BOOT. For this reason, it is highly recommended to use the new Firmware Upgrade script whenever you need to download new firmware to the MCE.

2. For the rest of the Upgrade Procedure, please see the detailed upgrade document *FirmwareUpgrade.pdf*. This document can be opened from the script view in ServiceShell by right-clicking on the Firmware Upgrade script, and clicking Help for selected script. Then click the link to the pdf file:



The *FirmwareUpgrade.pdf* file can also be found in the d:\ServiceShell\Scripts\device folder.

3. VERSION HISTORY

00.03	early release
00.04	remove scsi.rst, and eh output from IO scanners, 2b backwards compatible with mce1 code (removed from IOS)
00.05	invert home and away as read in carriage status reg. (unchanged in IOS)
00.06	fixes a bus alignment problem introduced in 0.04. also better dsack gen. To allow reliable sram writes
00.07	add dp debug test points
00.08	fix a comparator in fdpe_4
00.09	add test points to 0.08 for diagnostic purposes only
00.10	add another test point

00.11	fix logicblox problem
00.13	fixes drum problem
00.14	adds delay stage to ct_buffer read addr.
00.20	fix several plot artifacts
00.21	Bill Dall - changed EDGE_SIM SM in many ways...
00.28	latest release
00.31	source reorganized
00.37	pause bit added to 0xc02234 bit 7
00.40	add drs watchdog, and restore debug register
00.50	add pause bit cpu I/F and tach modules vhdl
00.55	added address irq support, converted pll to vhdl
00.60	converted irq and plt modules to vhdl, fixed drum amp analog output
00.80	add Lotem800 features incl. rotation count, postition latching and drum drive direction control
00.85	fixed bug in lotem TSP interface.
00.90	update to new pll and new mpc fw support fixed drs end_cycle bug, and pll seed/overflow-underflow bug
00.92	Includes changes to tach module that allow flexibility with types of encoders used.
00.96	Fix TSP 'missing data' artifact
00.97	Better fix the missing data artifact
00.98	update to new carriage
00.99	Supports proofing

01.01	updates to crg (bigger pos register, safety limit support, blank skip support)
01.02	(gregh) 18/Jul/2001 In DP, pp. 5, 6 and 8 are all VHDL. No functional changes.
01.03	(mikehollin) 9/aou/2001 Add the lower three bits to the lpr product and add to more bits to sfpr
01.05	(mikehollin) 29/aou/2001 Added new registers to test tsp board level signals.
01.25	(gregh) 09/jan/2001 Changes since 1.05 include: gapless support, new fdp_di_cont input state machine, robust tsp_fifo, pin changes for hydra, fixed master-slave sync for hydra, CRC to check data flow between datapath and head, CRCs to check TSP data, hydra slave and master edge detect, hydra can set and clear multi-head mode without resetting system.
01.32	(GHall) 22/fev/2002 Exactly the same as 1.25 except includes the image inversion ability with patterns.
01.33	(GHall) 12/mar/2002 Includes fixes for Hydra, TSP communication, and image inversion with patterns.
01.36	(GHall) 29/mai/2002 Includes fixes for Hydra and TSP communication (mainly improving timing of TSP-TMCE signals)
01.37	(GHall) 29/mai/2002 Same as 1.36 except for uses more efficient time constraints in UCF file. All paths are constrained.
01.38	(GHall) 12/aou/2002 Contains improved 1200 DPI staircase fix.
01.39	(GHall) Dec/2003 Released as patch for 01.37 but bugs found. DO NOT USE.
01.40	(MHollingsh) 23/aou/2002 Fix the problem with the gong that occurred when the pll was enabled.
01.41	(GHall) Jan/28/2004 Patch for 01.37 that works. Includes new FIFO for TSP interface to reduce timing issues. Also, resetting input buffers and FIFO on each packet to eliminate horizontal data shift errors.
01.50	(GHall) 11/dec/2002 8-neighbour pixel scrubbing added.
01.65	(MHollingsh) 28/jan/2003 merged pixel scrubbing with pll_enable fix. Added pixel counting.

	Part Number: 636-00022A-A
01.67	(GHall) Dec/2003 Released as patch for 01.65 to resolve TSP issues but bugs found. DO NOT USE.
01.68	(GHall) Jan/28/2004 Patch for 01.65 that works. Includes new FIFO for TSP interface to reduce timing issues. Also, resetting input buffers and FIFO on each packet to eliminate horizontal data shift errors.
01.69	(GHall) 24/avr/2003 Special Manta release only: Added SCSI CRC and merged crg at slow drum speed changes in (required CRG fmw version 1.44 or better)
01.70	(GHall) 24/avr/2003 Added SCSI CRC and merged crg at slow drum speed changes in (required CRG fmw version 1.44 or better). Meets all timing and available for all machines.
01.76	(GHall) 25/juin/2003 - Added dot reduction, Added pixel scrubbing, Added PLL Status bit, Fixed a cross-clock-domain metastability problem. Part number: TBD
01.77	(GHall) 30/juil/2003 - Fixed problem with dot reduction and pixel scrubbing generating artifacts with overwriting patterns. Moved collison bit from bit 2 to bit 3 of GenInputs 1. Part Number: 636-00033A-A
01.79	(GHall) 05/sept/2003 - Added the ability to use the edge signal to latch drum and carriage values into the generic latches. Part Number: 636-00037A-A
01.84	(GHall) Dec/2003 - Released with some fixes but bugs found. DO NOT USE.
01.86	(GHall) Dec/2003 - Added ability to do slave-only plots on hydra machines.
01.87	Jan 28, 2004 (GHall) - Connected spare bit on the drum amp connector (MD_SP_OUT) to drum watchdog. MD.SP_OUT is bit 7 of the GenOutputs1 register at xC02420. - Restored a fix for gravure that was included in FDP_DI_CONT.vhd of the datapath in version 1.33 of the baseline then accidentally eliminated. The fix was for a problem where specific image sizes would hang due to a math error in the Xilinx. - Added new TSP FIFOs - Now using standard FIFOs from coregen which

	should eliminate any metastability issues and 5230 errors on Brisque. Also, resetting these FIFOs and the input buffer counter on each packet to eliminate the horizontal data artifact problem. Part Number: 636-00074A
01.94	March 8, 2004 (GHall) - Added blank skip support - improved pixel counting algorithm - increased register sizes in PLL to allow for locking above 950 RPM. Part Number: 636-00075A
02.11	May 11, 2004 (GHall) - Blank skip ability improved - Pixel counting algorithm implementation fixed. - update_ortho_reg routed out as an interrupt - increase imageSize reg to 21 bits - add lmce_ti_en to crg - Changes transparent to firmware: move te_en up to top level, made pif more generic Part Number: 636-00087A
02.23	September 14, 2004 (GHall) - Increased TSP registers scanline_count and scanline_progress to 24 bits - added fix to dp_ext_gate_select to fix slave-master issue in Hydra. Slave can now be designated as a slave and plot in master-slave mode as well as slave-only mode. - made TSP clock detection circuit less sensitive to frequency fluctations. Should help resolve "Data Channel Not Detected" errors. Part Number: 636-00093A