MICROCONTROLLER UNIT
MCU.SCH

MCU,
DATA BUS LEVEL TRANSLATORS.

SHEET 2

DATAPATH
DATAPATH.SCH

OCCT SDRAM,
TPG SRAM,
HOTLINK.

SHEET 7

TEMPERATURE SENSORS
TEMP.SCH

THERMISTOR INTERFACE,
REFERENCE VOLTAGE,
SPARE ANALOG INPUT.

SHEET 12

DIGITAL SENSORS 4
DSENSE4.SCH

LOW VOLTAGE DETECT,
ELECTRONIC REGISTRATION.

SHEET 17

POWER SWITCHERS
SWITCHER.SCH

+5V SWITCHER,
+12V SWITCHER,
-12V SWITCHER,
+3.3V REGULATOR,
+2.5V REGULATOR.

SHEET 22

POWER SUPPLY 1
POWER1.SCH

POWER SUPPLY OF
SHEET 2 TO SHEET 5.

SHEET 24

ADDRESS DECODING
CPLD.SCH

CPLD,
RESET MONITOR,
VERSION REGISTERS,
SPI CLOCK BUFFER.

SHEET 3

HEAD INTERFACE AND HOME AND AWAY
HEADIF.SCH

HEAD INTERFACE
HOME AND AWAY INTERFACE

SHEET 8

PRESSURE SENSORS
PRESSURE.SCH

PRESSURE SENSORS,
A/D CONVERTER.

SHEET 13

DIGITAL SENSORS 5
DSENSE5.SCH

6 OPTO-INTERRUPTER INTERFACE,
DSUB25F CONNECTOR.

SHEET 18

LOGIC ANALYZER HEADERS
LAH.SCH

LOGIC ANALYZER HEADERS.

SHEET 23

POWER SUPPLY 2
POWER2.SCH

POWER SUPPLY OF
SHEETS 6, 7, AND 28.

SHEET 25

MEMORY
MEMORY.SCH

FLASH,
SRAM,
NVRAM,
BMM CONNECTOR.

SHEET 4

SERIAL COMMUNICATION PORTS
UART.SCH

QUAD UART,
RS-232 TRANSCEIVERS,
DONGLE PORT,
PLATE PROCESSOR (SPARE) PORT,
WORKSTATION PORT,
DIAG PORT.

SHEET 9

DIGITAL SENSORS 1
DSENSE1.SCH

9 OPTO-INTERRUPTER INTERFACE,
DSUB37F CONNECTOR.

SHEET 14

DRIVERS
DRIVERS.SCH

SOLENOID DRIVERS,
SPARE AND USER ALARM RELAY DRIVERS,
USER INTERFACE.

SHEET 19

POWER SUPPLY 3
POWER3.SCH

POWER SUPPLY OF
SHEET 8 TO SHEET 16.

SHEET 26

EXPOSURE HEAD INTERFACE
FPGA.SCH

MICRO INTERFACE TO FPGA,
OSCILLATORS.

SHEET 5

TACH AND DRUM AMP
DRUM.SCH

TACH ENCODER,
DRUM AMP INTERFACE.

SHEET 10

DIGITAL SENSORS 2
DSENSE2.SCH

9 OPTO-INTERRUPTER INTERFACE,
DSUB37M CONNECTOR.

SHEET 15

MISCELANEOUS I/O
MISCIO.SCH

LEDS,
CARRIAGE AMP POWER CONNECTOR,
JTAG PORT,
GROUND TEST POINTS,
MOUNTING HOLES.

SHEET 20

POWER SUPPLY 4
POWER4.SCH

POWER SUPPLY OF
SHEET 17 TO SHEET 21.

SHEET 27

FAST DATAPATH ELECTRONICS
SCSI.SCH

SCSI CONNECTOR,
SCSI TERMINATORS,
SCSI DRIVERS,
SCSI CONTROLLER.

SHEET 6

CARRIAGE AMP INTERFACE
CARRIAGE.SCH

CARRIAGE AMP INTERFACE.

SHEET 11

DIGITAL SENSORS 3
DSENSE3.SCH

2 OPTO-INTERRUPTER (RJ45),
LOAD RAMP SENSOR,
PLATE FLYOFF SENSOR.

SHEET 16

EXPANSION BUS
EXPBUS.SCH

EXPANSION BUS (SCON) CONNECTORS,
CAN TRANSCEIVER.

SHEET 21

TURBOSCREENING
TURBOSCR.SCH

PECL-TTL CONVERTERS
TTL-PECL CONVERTERS
TURBOSCREENING CONNECTOR

SHEET 28

EDGE DETECTION
EDGE.SCH

EDGE DETECTION FOR
FIBRE HEAD MACHINES
(connector on page 12)

SHEET 29

creo Turbo Master Control Electronics

C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\Mce.prj

DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	October 23, 2002	1 of 29

BUS LEVEL SHIFTERS

U22A — 74VHCT245A,TSSOP20

U31A — 74VHCT245A,TSSOP20

MICROCONTROLLER

U37A — MC68376

Note: MC68376 requires the pull-down resistor be sized such that a valid low results from the reset mode input current of 120 uA. (MC68376 User's Manual, Page A-4) This is needed to enable A19-A23.

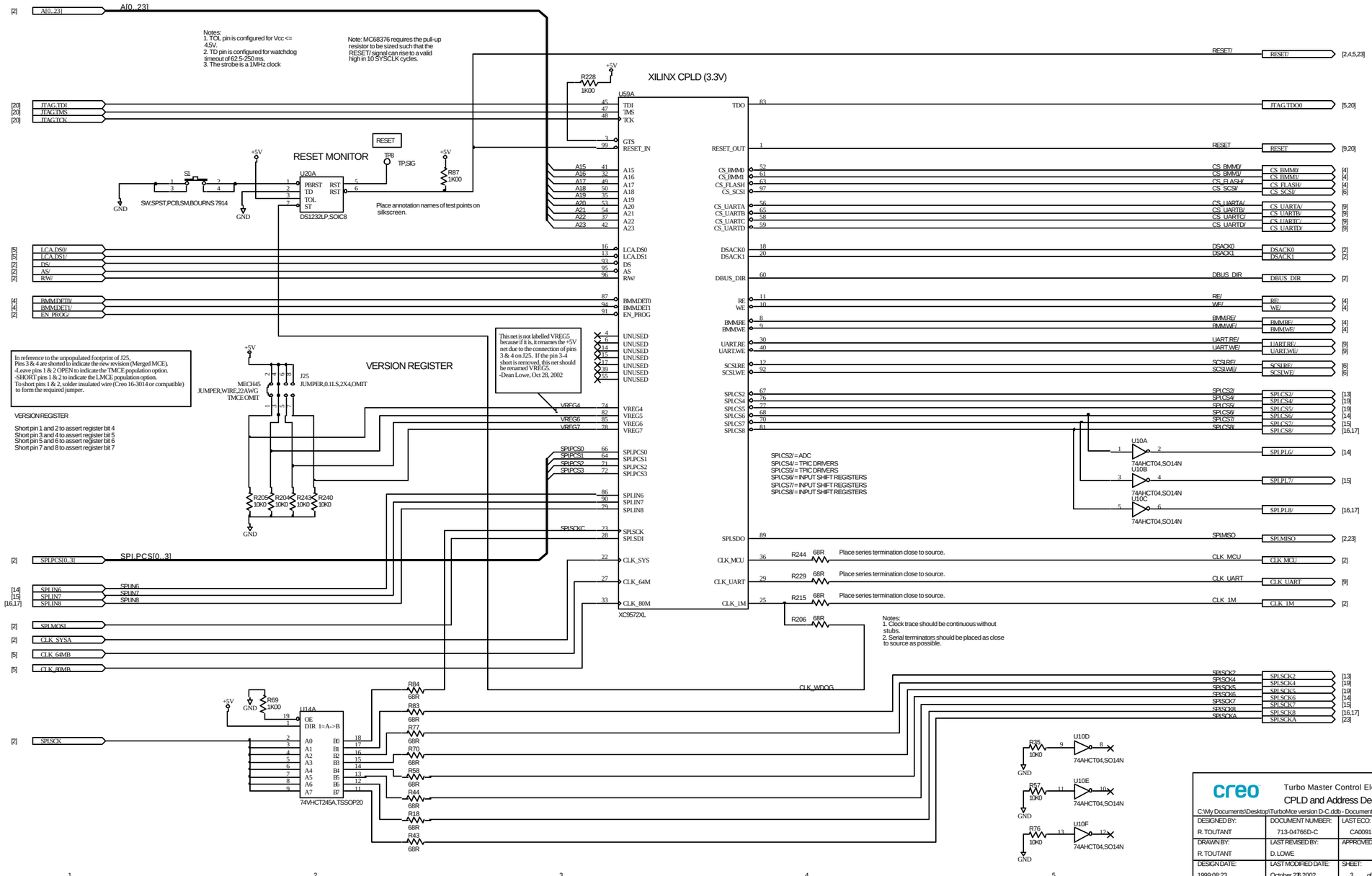
BOOT JUMPER/PUSHBUTTON

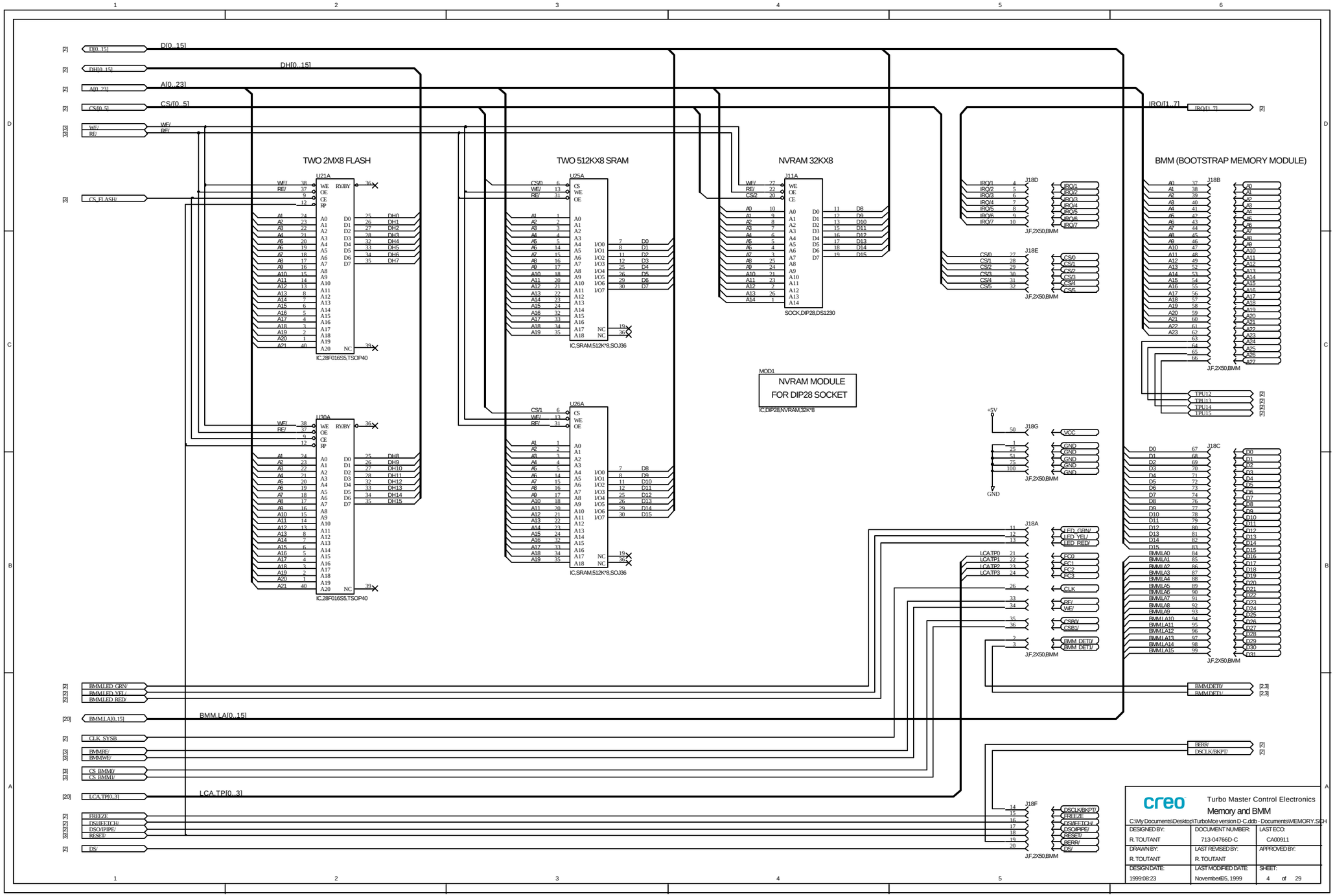
Short out jumper to force firmware to start up in boot mode.

Place series termination close to source.

Notes:
1. Clock trace should be continuous without stubs.
2. Serial terminators should be placed as close to source as possible.

creo	Turbo Master Control Electronics
	Microcontroller
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\MCU.SCH	
DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911	
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE
APPROVED BY:	
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 23, 2002
SHEET: 2 of 29	


A[0..23]
Notes:
1. TOL pin is configured for Vcc <= 4.5V.
2. TD pin is configured for watchdog timeout of 62.5-250 ms.
3. The strobe is a 1MHz clock
Note: MC68376 requires the pull-up resistor to be sized such that the RESET signal can rise to a valid high in 10 SYSCLK cycles.
XILINX CPLD (3.3V)
U59A
RESET MONITOR
SW,SPST,PCB,SM,BOURNS 7914
DS1232LP,SOIC8
U20A
Place annotation names of test points on silkscreen.
In reference to the unpopulated footprint of J25.
Pins 3 & 4 are shorted to indicate the new revision (Merged MCE).
-Leave pins 1 & 2 OPEN to indicate the TMCE population option.
-SHORT pins 1 & 2 to indicate the LMCE population option.
To short pins 1 & 2, solder insulated wire (Creo 16-3014 or compatible) to form the required jumper.
VERSION REGISTER
Short pin 1 and 2 to assert register bit 4
Short pin 3 and 4 to assert register bit 5
Short pin 5 and 6 to assert register bit 6
Short pin 7 and 8 to assert register bit 7
VERSION REGISTER
MECH45
JUMPER,WIRE,22AWG
TMCE OMIT
J25
JUMPER,0.1LS,2X4,OMIT
This net is not labelled VREG5 because if it is, it renames the +5V net due to the connection of pins 3 & 4 on J25. If the pin 3-4 short is removed, this net should be renamed VREG5.
-Dean Lowe, Oct 28, 2002
SPI_PCS[0..3]
U14A
74VHCT245A,TSSOP20
XC9572XL
Notes:
1. Clock trace should be continuous without stubs.
2. Serial terminators should be placed as close to source as possible.
U10A
U10B
U10C
U10D
U10E
U10F
74AHCT04,SO14N
SPLCS2/= ADC
SPLCS4/= TPIC DRIVERS
SPLCS5/= TPIC DRIVERS
SPLCS6/= INPUT SHIFT REGISTERS
SPLCS7/= INPUT SHIFT REGISTERS
SPLCS8/= INPUT SHIFT REGISTERS
Place series termination close to source.
creo
Turbo Master Control Electronics
CPLD and Address Decoding
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\CPLD.SCH
DESIGNED BY: R. TOUTANT
DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911
DRAWN BY: R. TOUTANT
LAST REVISED BY: D. LOWE
APPROVED BY:
DESIGN DATE: 1999:08:23
LAST MODIFIED DATE: October 25 2002
SHEET: 3 of 29

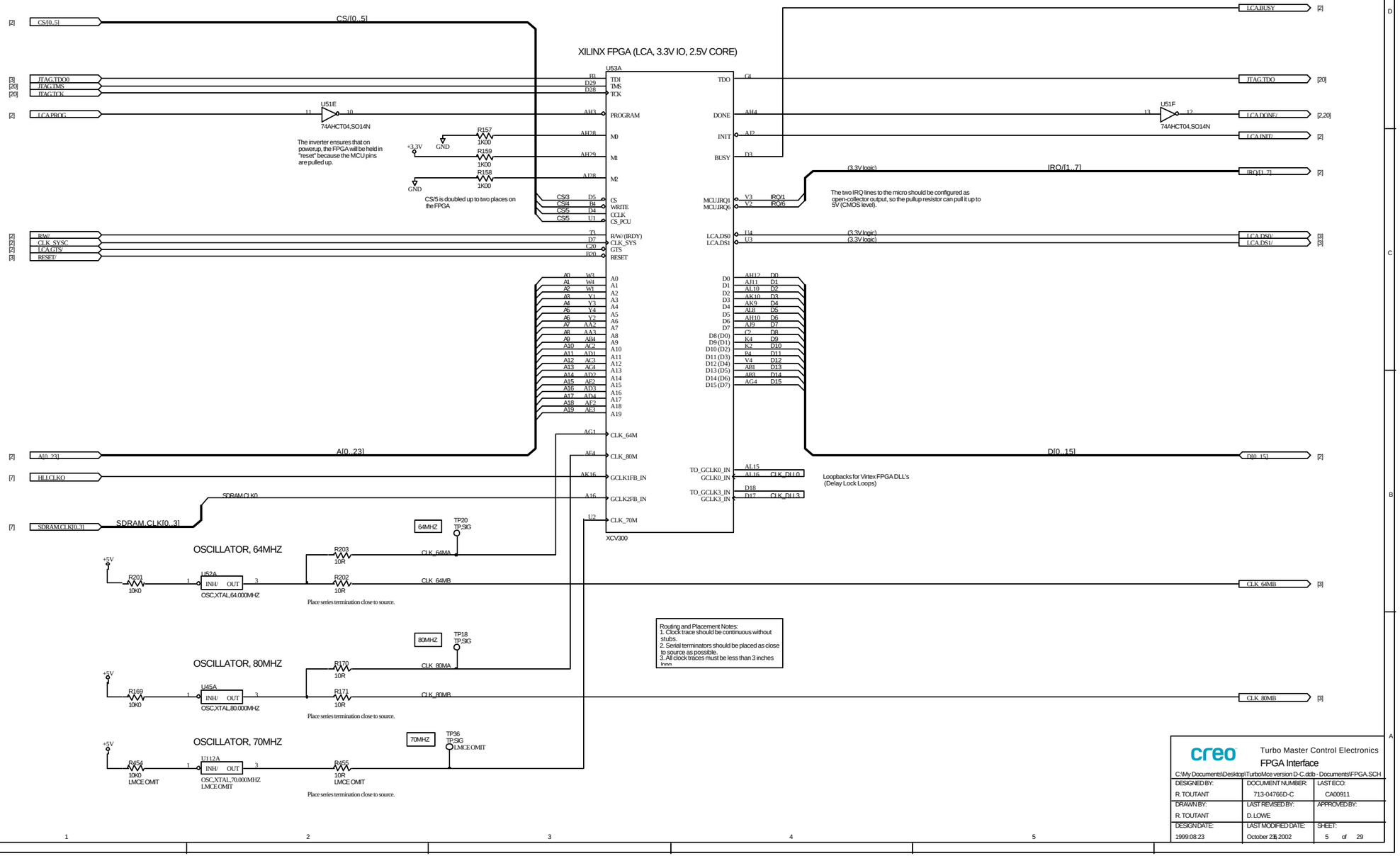


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Memory and BMM

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R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	R. TOUTANT	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	November 05, 1999	4 of 29


XILINX FPGA (LCA, 3.3V IO, 2.5V CORE)
U53A
XCV300
CS/[0..5]
A[0..23]
D[0..15]
SDRAM.CLK[0..3]
JTAG.TDO0
JTAG.TMS
JTAG.TCK
LCA.PROG
HLI.CLKO
RAW
CLK_SYSC
LCA.GTS/
RESET/
TDI
TMS
TCK
PROGRAM
M0
M1
M2
CS
WRITE
CCLK
CS_PCU
R/W/(IRDY)
CLK_SYS
GTS
RESET
CLK_64M
CLK_80M
GCLK1FB_IN
GCLK2FB_IN
CLK_70M
TDO
DONE
INIT
BUSY
MCU.IRQ1
MCU.IRQ6
LCA.DS0
LCA.DS1
TO_GCLK0_IN
GCLK0_IN
TO_GCLK3_IN
GCLK3_IN
CLK_DLL0
CLK_DLL3
U51E
74AHCT04,SO14N
U51F
74AHCT04,SO14N
R157
R159
R158
1K00
The inverter ensures that on powerup, the FPGA will be held in "reset" because the MCU pins are pulled up.
CS/5 is doubled up to two places on the FPGA
(3.3V logic)
IRQ/[1..7]
The two IRQ lines to the micro should be configured as open-collector output, so the pullup resistor can pull it up to 5V (CMOS level).
(3.3V logic)
Loopbacks for Virtex FPGA DLL's (Delay Lock Loops)
LCA.BUSY
JTAG.TDO
LCA.DONE/
LCA.INIT/
IRQ/[1..7]
LCA.DS0/
LCA.DS1/
D[0..15]
CLK_64MB
CLK_80MB
OSCILLATOR, 64MHZ
OSCILLATOR, 80MHZ
OSCILLATOR, 70MHZ
64MHZ
80MHZ
70MHZ
TP20
TP18
TP36
TP.SIG
LMCE OMIT
CLK_64MA
CLK_64MB
CLK_80MA
CLK_80MB
U52A
U45A
U112A
OSC,XTAL,64.000MHZ
OSC,XTAL,80.000MHZ
OSC,XTAL,70.000MHZ
R201
R202
R203
R169
R170
R171
R454
R455
10K0
10R
+5V
GND
Place series termination close to source.
Routing and Placement Notes:
1. Clock trace should be continuous without stubs.
2. Serial terminators should be placed as close to source as possible.
3. All clock traces must be less than 3 inches long.
creo
Turbo Master Control Electronics
FPGA Interface
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\FPGA.SCH
DESIGNED BY: R. TOUTANT
DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911
DRAWN BY: R. TOUTANT
LAST REVISED BY: D. LOWE
APPROVED BY:
DESIGN DATE: 1999:08:23
LAST MODIFIED DATE: October 25 2002
SHEET: 5 of 29

LVD TERMINATORS

SCSI CONTROLLER LVD I/F

SCSI BUS CONTROLLER

XILINX FPGA

A[0..23]

D[0..15]

CS_SCSI/

SCSIRF/

SCSIWE/

SCSI CONN, LVD P, VERT
LMCE OMIT

TERM,SCSI,UCC5672PWP
LMCE OMIT

DIFFSENS_FILT

DIFFSENS

FAS368M
LMCE OMIT

FAS368M
LMCE OMIT

XCV300

Differential SCSI Routing (with a "+" or a "-" at the end of the net name on this page):

- Route all differential SCSI connections using 6 mil trace width and 6 mil spacing between a differential pair (eg. DB0+ and DB0- are separated by 6 mils).
- Equalize net lengths of each differential pair to within 50 mils, and equalize net lengths between different differential pairs to within 500 mils.
- Keep separation between adjacent differential pairs to at least 12 mils (on the same layer).

SCSI terminators should be placed close to the SCSI connector.

TERMPWR is generated on sheet 25

100Hz Input LPF for filtering

Pull DIFFM down with 50 Ohm resistor

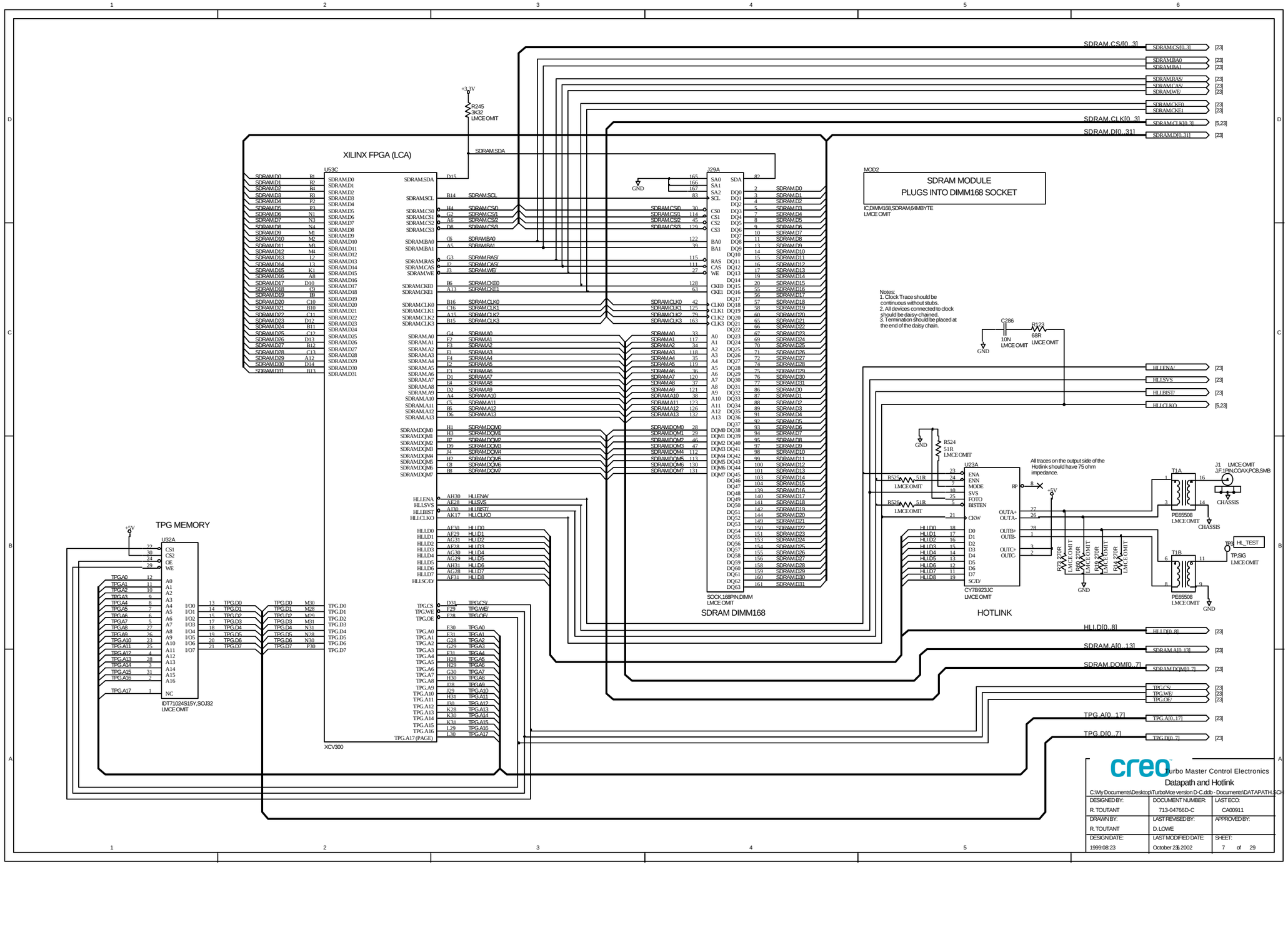
Place terminators close to the end of the daisy chain (at the FAS368M or the logical analyzer headers on Page 22).

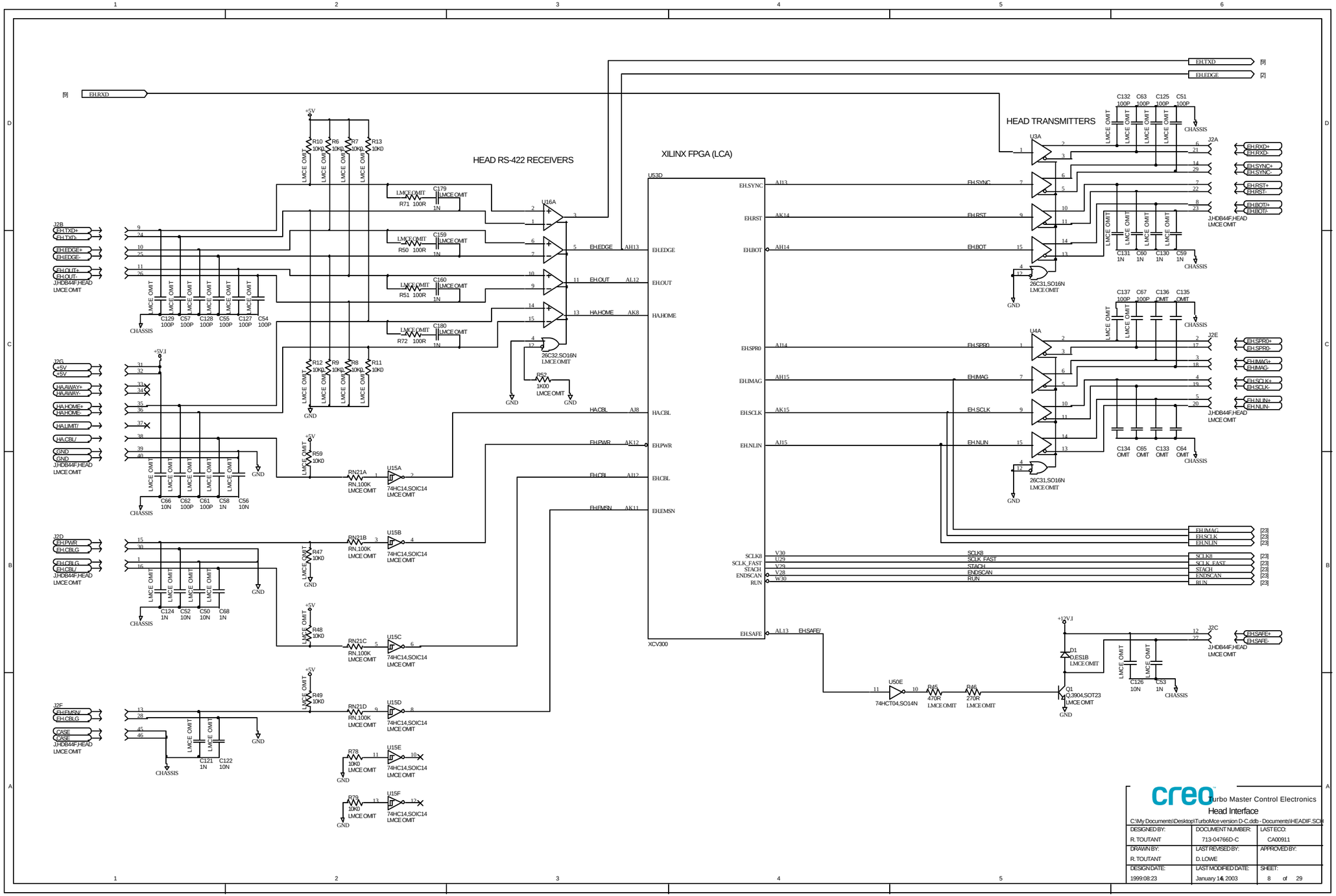
"SCSI.*" routing:

Equalize all "SCSI.*" net lengths to within 500 mils. Component connections should be daisy-chained.

Attach spacers (aka jack screws), nuts, and lock washers into mounting holes of J42

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	SCSI Controller Interface		
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\SCSI.SCH			
DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911	
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:	
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: January 15, 2003	SHEET: 6 of 29	


SDRAM.CS/[0..3]
SDRAM.CS[0..3] [23]
SDRAM.BA0 [23]
SDRAM.BA1 [23]
SDRAM.RAS/ [23]
SDRAM.CAS/ [23]
SDRAM.WE/ [23]
SDRAM.CKE0 [23]
SDRAM.CKE1 [23]
SDRAM.CLK[0..3]
SDRAM.CLK[0..3] [5,23]
SDRAM.D[0..31]
SDRAM.D[0..31] [23]
+3.3V
R245
3K32
LMCE OMIT
SDRAM.SDA
XILINX FPGA (LCA)
U53C
SDRAM.D0 R1
SDRAM.D1 R2
SDRAM.D2 R4
SDRAM.D3 R3
SDRAM.D4 P2
SDRAM.D5 P3
SDRAM.D6 N1
SDRAM.D7 N3
SDRAM.D8 N4
SDRAM.D9 M1
SDRAM.D10 M2
SDRAM.D11 M5
SDRAM.D12 M4
SDRAM.D13 L2
SDRAM.D14 L3
SDRAM.D15 K1
SDRAM.D16 A8
SDRAM.D17 D10
SDRAM.D18 C9
SDRAM.D19 B9
SDRAM.D20 C10
SDRAM.D21 B10
SDRAM.D22 C11
SDRAM.D23 D12
SDRAM.D24 B11
SDRAM.D25 C12
SDRAM.D26 D13
SDRAM.D27 B12
SDRAM.D28 C13
SDRAM.D29 A12
SDRAM.D30 D14
SDRAM.D31 B13
SDRAM.SDA D15
SDRAM.SCL B14
SDRAM.CS0 H4
SDRAM.CS1 G2
SDRAM.CS2 A6
SDRAM.CS3 D8
SDRAM.BA0 G5
SDRAM.BA1 A5
SDRAM.RAS G3
SDRAM.CAS F2
SDRAM.WE J3
SDRAM.CKE0 B5
SDRAM.CKE1 A13
SDRAM.CLK0 B16
SDRAM.CLK1 C16
SDRAM.CLK2 A15
SDRAM.CLK3 B15
SDRAM.A0 G4
SDRAM.A1 F2
SDRAM.A2 F3
SDRAM.A3 F1
SDRAM.A4 F4
SDRAM.A5 E2
SDRAM.A6 E3
SDRAM.A7 D1
SDRAM.A8 E4
SDRAM.A9 D2
SDRAM.A10 A4
SDRAM.A11 C5
SDRAM.A12 B5
SDRAM.A13 D6
SDRAM.DQM0 H1
SDRAM.DQM1 H3
SDRAM.DQM2 B2
SDRAM.DQM3 D3
SDRAM.DQM4 J4
SDRAM.DQM5 H2
SDRAM.DQM6 C1
SDRAM.DQM7 B1
HLLENA AH30
HLLSVS AE28
HLLBIST AJ30
HLLCLKO AK17
HLLD0 AF30
HLLD1 AF29
HLLD2 AG31
HLLD3 AE28
HLLD4 AG30
HLLD5 AG29
HLLD6 AH31
HLLD7 AG28
HLLSC/DY AF31
TPG.CS AD31
TPG.WE AE29
TPG.OE AE28
TPG.A0 AE30
TPG.A1 AE31
TPG.A2 G28
TPG.A3 G29
TPG.A4 E31
TPG.A5 H28
TPG.A6 H29
TPG.A7 G30
TPG.A8 H30
TPG.A9 D28
TPG.A10 J29
TPG.A11 H31
TPG.A12 D30
TPG.A13 K28
TPG.A14 K30
TPG.A15 K31
TPG.A16 L29
TPG.A17 (PAGE) L30
XCV300
J29A
SDA 82
SA0 165
SA1 166
SA2 167
SCL 83
GND
SDRAM.CS0 30
SDRAM.CS1 114
SDRAM.CS2 45
SDRAM.CS3 129
122
99
115
111
27
128
63
SDRAM.CLK0 42
SDRAM.CLK1 125
SDRAM.CLK2 79
SDRAM.CLK3 163
SDRAM.A0 33
SDRAM.A1 117
SDRAM.A2 34
SDRAM.A3 118
SDRAM.A4 35
SDRAM.A5 119
SDRAM.A6 36
SDRAM.A7 120
SDRAM.A8 37
SDRAM.A9 121
SDRAM.A10 38
SDRAM.A11 123
SDRAM.A12 126
SDRAM.A13 132
SDRAM.DQM0 28
SDRAM.DQM1 29
SDRAM.DQM2 46
SDRAM.DQM3 47
SDRAM.DQM4 112
SDRAM.DQM5 113
SDRAM.DQM6 130
SDRAM.DQM7 131
SOCK.168PIN.DIMM
LMCE OMIT
SDRAM DIMM168
MOD2
SDRAM MODULE
PLUGS INTO DIMM168 SOCKET
IC.DIMM168.SDRAM.64MBYTE
LMCE OMIT
Notes:
1. Clock Trace should be continuous without stubs.
2. All devices connected to clock should be daisy-chained.
3. Termination should be placed at the end of the daisy chain.
C286
10N
LMCE OMIT
R123
68R
LMCE OMIT
HLLENA/ [23]
HLLSVS [23]
HLLBIST/ [23]
HLLCLKO [5,23]
R524
51R
LMCE OMIT
U23A
R525 51R LMCE OMIT
R526 51R LMCE OMIT
ENA
ENN
MODE
SVS
FOTO
BISTEN
CKW
D0
D1
D2
D3
D4
D5
D6
D7
SCD/
OUTA+
OUTA-
OUTB+
OUTB-
OUTC+
OUTC-
CY7B923JC
LMCE OMIT
HLLD0 18
HLLD1 17
HLLD2 16
HLLD3 15
HLLD4 14
HLLD5 13
HLLD6 12
HLLD7 11
HLLD8 19
All traces on the output side of the Hotlink should have 75 ohm impedance.
R527 270R LMCE OMIT
R528 270R LMCE OMIT
R529 270R LMCE OMIT
R534 270R LMCE OMIT
J1 LMCE OMIT
JF.1PIN.COAX.PCB.SMB
CHASSIS
T1A
T1B
PE65508
LMCE OMIT
TP9 HL_TEST
TP.SIG
LMCE OMIT
HLLD[0..8]
HLLD[0..8] [23]
SDRAM.A[0..13]
SDRAM.A[0..13] [23]
SDRAM.DQM[0..7]
SDRAM.DQM[0..7] [23]
TPG.CS/ [23]
TPG.WE/ [23]
TPG.OE/ [23]
TPG.A[0..17]
TPG.A[0..17] [23]
TPG.D[0..7]
TPG.D[0..7] [23]
TPG.D0 M30
TPG.D1 M28
TPG.D2 M29
TPG.D3 M31
TPG.D4 N31
TPG.D5 N28
TPG.D6 N30
TPG.D7 P30
TPG MEMORY
U32A
TPG.A0 12
TPG.A1 11
TPG.A2 10
TPG.A3 9
TPG.A4 8
TPG.A5 7
TPG.A6 6
TPG.A7 5
TPG.A8 27
TPG.A9 26
TPG.A10 23
TPG.A11 25
TPG.A12 4
TPG.A13 28
TPG.A14 3
TPG.A15 31
TPG.A16 2
TPG.A17 1
IDT71024S15Y,SOJ32
LMCE OMIT
creo
Turbo Master Control Electronics
Datapath and Hotlink
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\DATAPATH.SCH
DESIGNED BY: R. TOUTANT
DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911
DRAWN BY: R. TOUTANT
LAST REVISED BY: D. LOWE
APPROVED BY:
DESIGN DATE: 1999:08:23
LAST MODIFIED DATE: October 25 2002
SHEET: 7 of 29



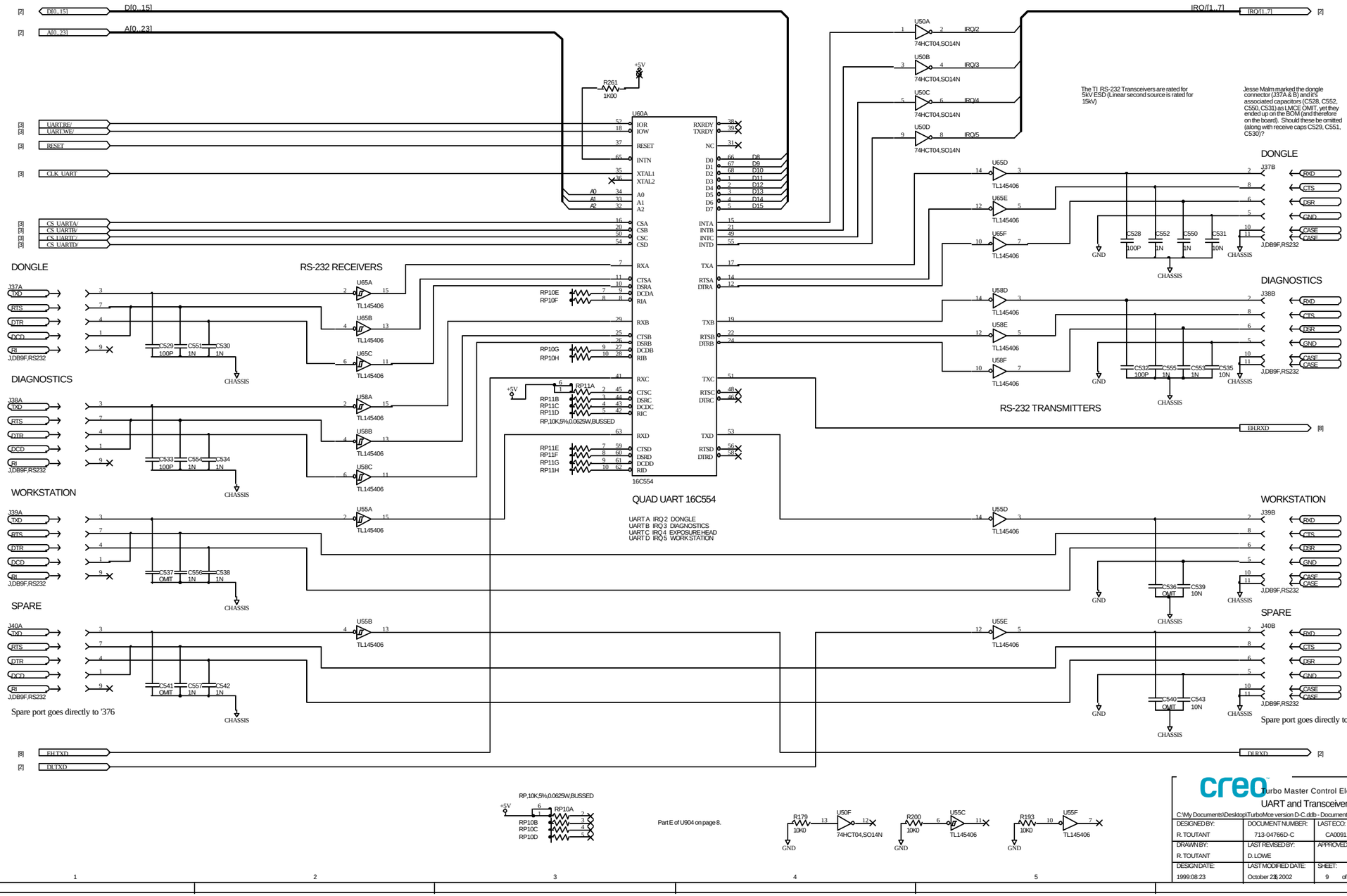
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Head Interface

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R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
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Part E of U904 on page 8.

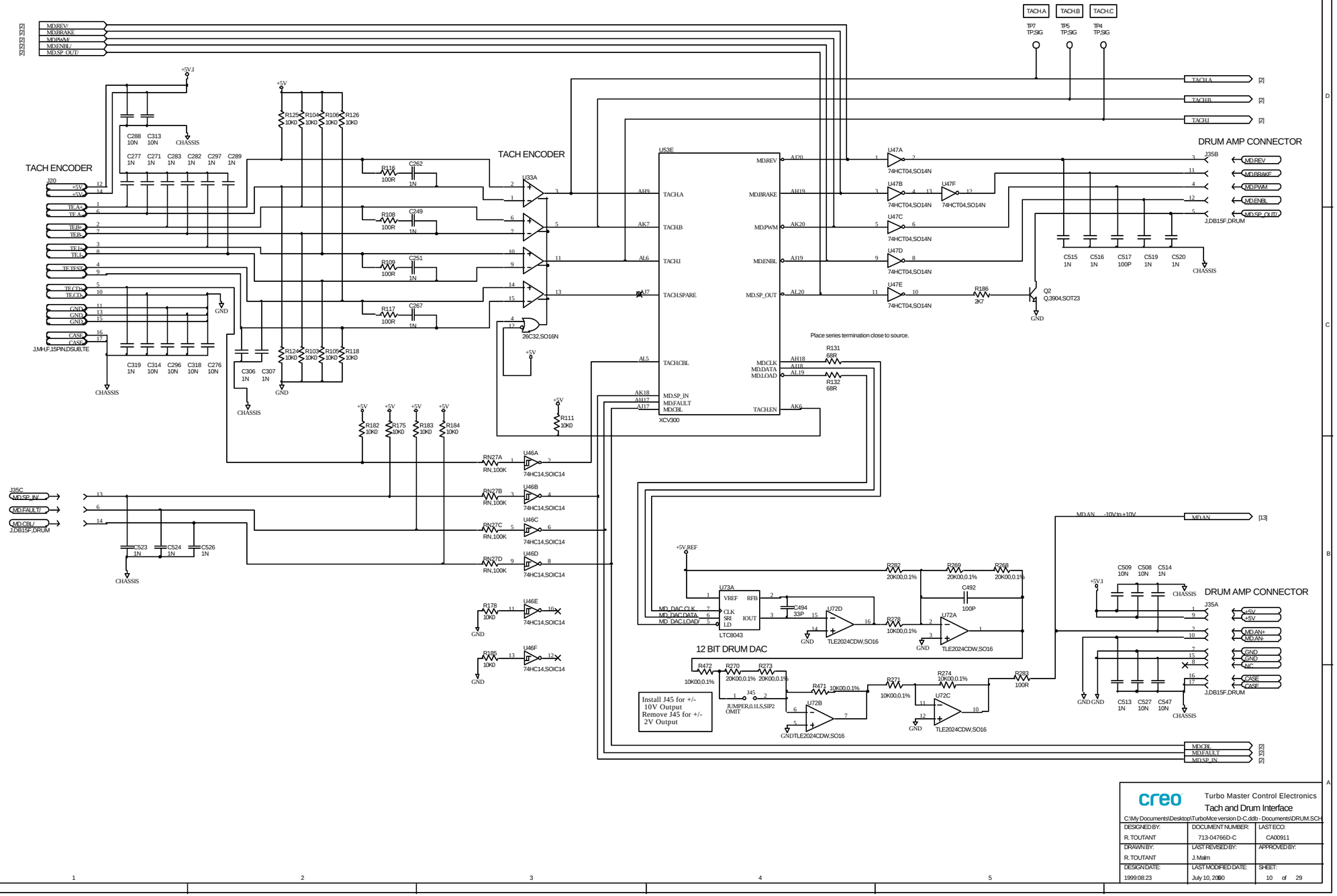
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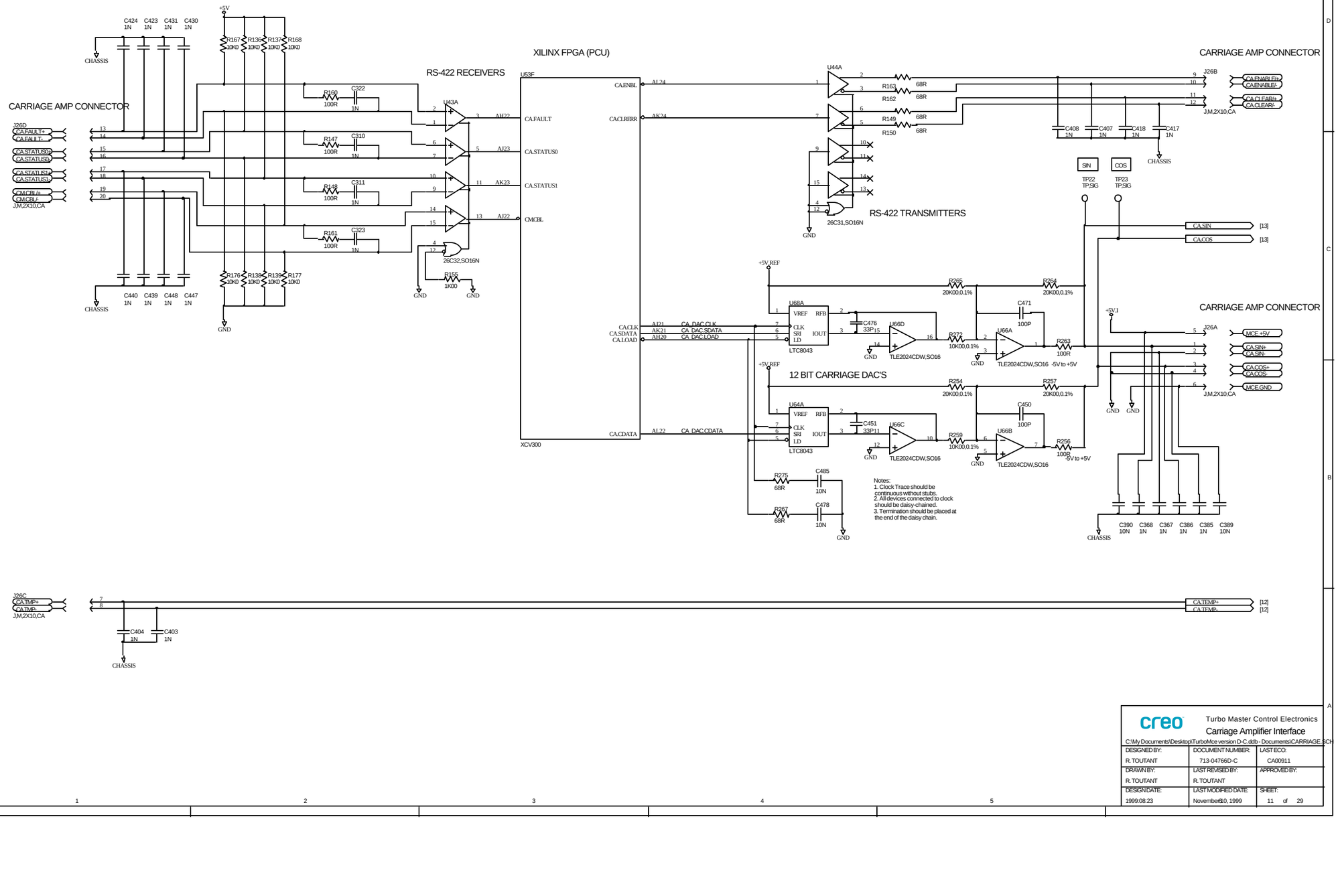
Turbo Master Control Electronics

UART and Transceivers

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DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 23, 2002	SHEET: 9 of 29


MD.REV/
MD.BRAKE
MD.PWM
MD.ENBL/
MD.SP_OUT/
TACH.A
TACH.B
TACH.I
TP7 TP.SIG
TP5 TP.SIG
TP4 TP.SIG
TACH ENCODER
J20
+5V
+5V
TE.A+
TE.A-
TE.B+
TE.B-
TE.I+
TE.I-
TE.TEST
TE.CD+
TE.CD-
GND
GND
GND
CASE
CASE
JMHF,15PIN,DSUB,TE
C288 10N
C313 10N
C277 1N
C271 1N
C283 1N
C282 1N
C297 1N
C289 1N
C319 1N
C314 10N
C296 10N
C318 10N
C276 10N
C306 1N
C307 1N
CHASSIS
GND
R125 10K0
R104 10K0
R106 10K0
R126 10K0
R124 10K0
R103 10K0
R105 10K0
R118 10K0
R116 100R
C262 1N
R108 100R
C249 1N
R109 100R
C251 1N
R117 100R
C267 1N
U33A
26C32,SO16N
TACH ENCODER
U53E
AH9 TACH.A
AK7 TACH.B
AL6 TACH.I
AL7 TACH.SPARE
AL5 TACH.CBL
AK18 MD.SP_IN
AH17 MD.FAULT
AJ17 MD.CBL
XCV300
MD.REV AJ20
MD.BRAKE AH19
MD.PWM AK20
MD.ENBL AJ19
MD.SP_OUT AL20
MD.CLK AH18
MD.DATA AH18
MD.LOAD AL19
TACH.EN AK6
Place series termination close to source.
R131 68R
R132 68R
R111 10K0
+5V
R182 10K0
R175 10K0
R183 10K0
R184 10K0
RN27A RN,100K
RN27B RN,100K
RN27C RN,100K
RN27D RN,100K
U46A 74HC14,SOIC14
U46B 74HC14,SOIC14
U46C 74HC14,SOIC14
U46D 74HC14,SOIC14
U46E 74HC14,SOIC14
U46F 74HC14,SOIC14
R178 10K0
R185 10K0
GND
J35C
MD.SP_IN/
MD.FAULT/
MD.CBL/
J.DB15F.DRUM
C523 1N
C524 1N
C526 1N
CHASSIS
U47A 74HCT04,SO14N
U47B 74HCT04,SO14N
U47C 74HCT04,SO14N
U47D 74HCT04,SO14N
U47E 74HCT04,SO14N
U47F 74HCT04,SO14N
R186 2K7
Q2 Q.3904,SOT23
DRUM AMP CONNECTOR
J35B
MD.REV
MD.BRAKE
MD.PWM
MD.ENBL
MD.SP_OUT
J.DB15F.DRUM
C515 1N
C516 1N
C517 100P
C519 1N
C520 1N
CHASSIS
[2]
[2]
[2]
[3]
[3]
[3]
+5V.REF
U73A
VREF RFB
CLK IOUT
SRI
LD
LTC8043
MD.DAC.CLK
MD.DAC.DATA
MD.DAC.LOAD
C494 33P
U72D
TLE2024CDW,SO16
R282 20K00,0.1%
R269 20K00,0.1%
R268 20K00,0.1%
C492 100P
R279 10K00,0.1%
U72A
TLE2024CDW,SO16
12 BIT DRUM DAC
R472 10K00,0.1%
R270 20K00,0.1%
R273 20K00,0.1%
R471 10K00,0.1%
R271 10K00,0.1%
R274 10K00,0.1%
R283 100R
U72B
U72C
TLE2024CDW,SO16
Install J45 for +/- 10V Output
Remove J45 for +/- 2V Output
JUMPER,0.11S,SIP2
OMIT
MD.AN -10V to +10V
MD.AN
[13]
C509 10N
C508 10N
C514 1N
C513 1N
C527 10N
C547 10N
DRUM AMP CONNECTOR
J35A
+5V
+5V
MD.AN+
MD.AN-
GND
GND
N/C
CASE
CASE
J.DB15F.DRUM
MD.CBL
MD.FAULT
MD.SP_IN
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Turbo Master Control Electronics
Tach and Drum Interface
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\DRUM.SCH
DESIGNED BY: R. TOUTANT
DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911
DRAWN BY: R. TOUTANT
LAST REVISED BY: J.Malm
APPROVED BY:
DESIGN DATE: 1999:08:23
LAST MODIFIED DATE: July 10, 2000
SHEET: 10 of 29


XILINX FPGA (PCU)
RS-422 RECEIVERS
RS-422 TRANSMITTERS
CARRIAGE AMP CONNECTOR
CARRIAGE AMP CONNECTOR
CARRIAGE AMP CONNECTOR
12 BIT CARRIAGE DAC'S
XCV300
LTC8043
TLE2024CDW,SO16
26C32,SO16N
26C31,SO16N
CA.FAULT
CA.STATUS0
CA.STATUS1
CM.CBL
CA.ENBL
CA.CLRERR
CA.CLK
CA.SDATA
CA.LOAD
CA.DATA
CA_DAC.CLK
CA_DAC.SDATA
CA_DAC.LOAD
CA_DAC.CDATA
CA.SIN
CA.COS
CA.TEMP+
CA.TEMP-
-5V to +5V
Notes:
1. Clock Trace should be continuous without stubs.
2. All devices connected to clock should be daisy-chained.
3. Termination should be placed at the end of the daisy chain.
Turbo Master Control Electronics
Carriage Amplifier Interface
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\CARRIAGE.SCH
DESIGNED BY: R. TOUTANT
DOCUMENT NUMBER: 713-04766D-C
LAST ECO: CA00911
DRAWN BY: R. TOUTANT
LAST REVISED BY: R. TOUTANT
APPROVED BY:
DESIGN DATE: 1999:08:23
LAST MODIFIED DATE: November 10, 1999
SHEET: 11 of 29

J46A
LMCF_Edge
GND
JDB9M,EDGE

J46B
NC
NC
JDB9M,EDGE

ANALOG_EDT_IN [29]

TEMPERATURE (ANALOG) SENSE CIRCUITS

[11] CA.TEMP+
[11] CA.TEMP-

+5V.REF

+12V.A
C452 100N
U62 REF02CS (Vin, +5V, TRIM, TEMP, GND)
C432 100N
U61A TLE2024CDW,SO16
R253 2K49
Q3 Q.3904,SOT23
R252 68R
R239 68R
TP21 TP.SIG
R260 10R
C441 22U

This device should not be used as a temperature sensor because the manufacturer(s) does not characterize the TEMP output for use as an accurate temp sensor.

LEADSCREW TEMP

R315 R,1K000
R370 R,22K00
R339 R,1K600
C410 10N
R319 R,100K0
R321 R,100K0
R320 R,100K0
U61B TLE2024CDW,SO16
R227 10K0
R340 R,1K000
R371 R,22K00
R317 R,1K600
R325 R,100K0
C425 10N

FRAME TEMP

R318 R,1K000
R372 R,22K00
R341 R,1K600
C411 10N
R324 R,100K0
R323 R,100K0
U61C TLE2024CDW,SO16
R225 10K0
R329 R,100K0
R346 R,1K000
R375 R,22K00
R338 R,1K600
R332 R,100K0
C419 10N

SPARE TEMP

R336 R,1K000
R376 R,22K00
R344 R,1K600
C426 10N
R334 R,100K0
R330 R,100K0
U61D TLE2024CDW,SO16
R226 10K0
R331 R,100K0
R377 R,22K00
R345 R,1K600
R333 R,100K0
R337 R,1K000
C427 10N

CARRIAGE TEMP

R316 R,1K000
R373 R,22K00
R342 R,1K600
C387 10N
R322 R,100K0
R326 R,100K0
R327 R,100K0
U56A TLE2024CDW,SO16
R211 10K0
TEMP.CA [13]
R374 R,22K00
R343 R,1K600
R335 R,1K000
R328 R,100K0
C370 10N

LOCAL TEMP

+5V.REF
R208 7K68
C369 10N
R210 22K1
U56B TLE2024CDW,SO16
R212 10K0
TEMP.LOCAL [13]
R207 1K00

TEMP.LS [13]
TEMP.PRM [13]
TEMP.SPARE [13]

J30B
TEMP0+
TEMP0-
TEMP1+
TEMP1-
TEMP2+
TEMP2-
JJM,MINIFIT,2X6,TEMP

C487 1N
C488 1N
C506 1N
C507 1N
C511 1N
C512 1N
CHASSIS

J46C
LSTEMP+
LSTEMP-
JDB9M,EDGE

C548 1N
C549 1N
CHASSIS

+5V.I

J30A
+5V
GND
PD.TEMP+
PD.TEMP-
NC
NC
JJM,MINIFIT,2X6,TEMP

C457 10N
C458 10N
C474 10N
C475 1N
CHASSIS
GND

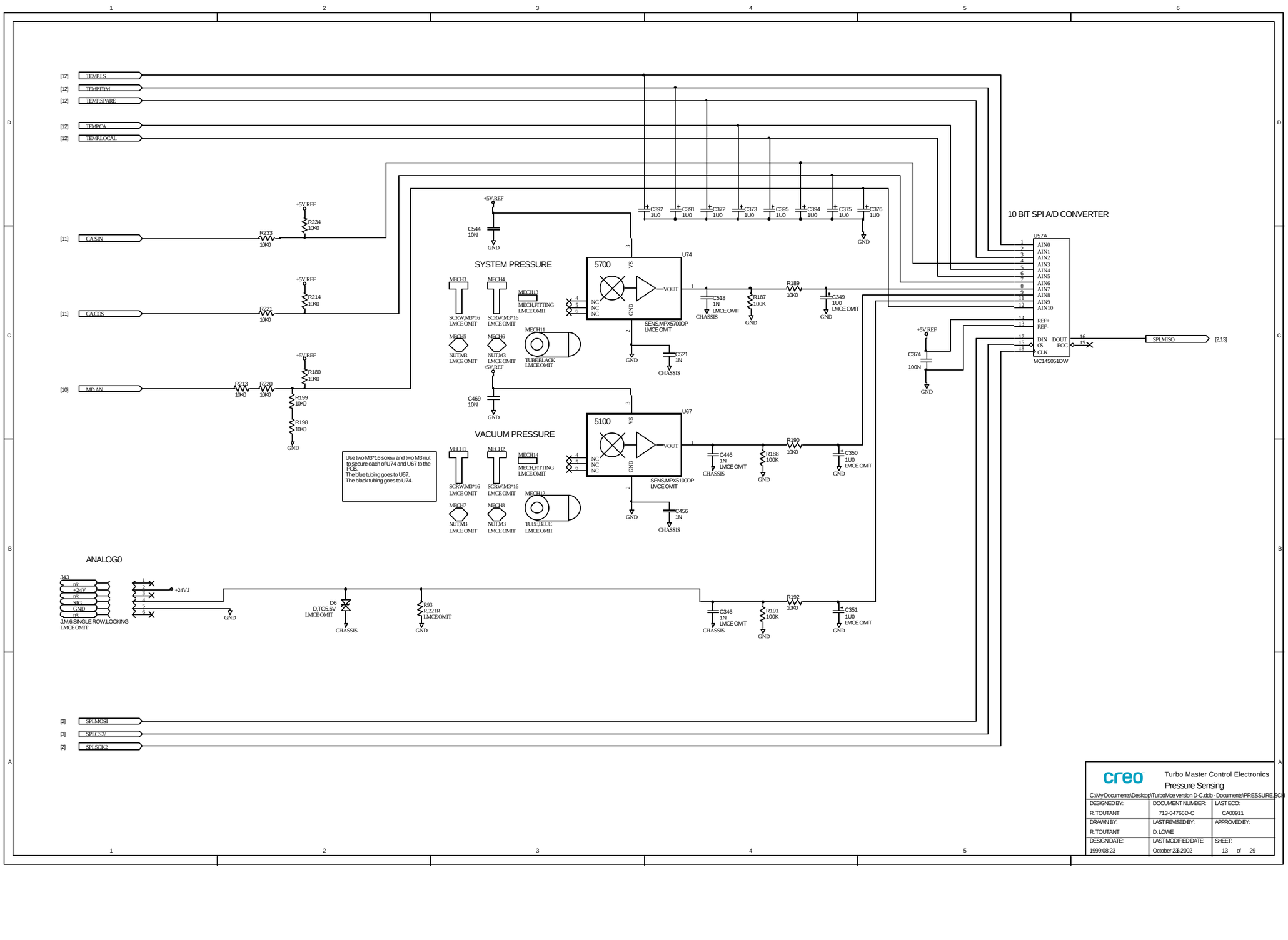
PD.TEMP [16]
PD.LSTEMP [16]

J46D
PD.LSTEMP+
PD.LSTEMP-
NC
JDB9M,EDGE

C545 10N
C546 1N
CHASSIS

U56C TLE2024CDW,SO16
U56D TLE2024CDW,SO16

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DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 25 2002	SHEET: 12 of 29



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Turbo Master Control Electronics

Pressure Sensing

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R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	October 25, 2002	13 of 29

DIGITAL SENSORS FOR ENDPLATE

[3] SPLSCK6
[3] SPLPL6/
[3] SPLCS6/

J4A DSEN0.LED+ DSEN0.LED- DSEN0.C DSEN0.E J,DB37F,DSENSE
J4B DSEN1.LED+ DSEN1.LED- DSEN1.C DSEN1.E J,DB37F,DSENSE
J4C DSEN2.LED+ DSEN2.LED- DSEN2.C DSEN2.E J,DB37F,DSENSE
J4D DSEN3.LED+ DSEN3.LED- DSEN3.C DSEN3.E J,DB37F,DSENSE
J4E DSEN4.LED+ DSEN4.LED- DSEN4.C DSEN4.E J,DB37F,DSENSE
J4F DSEN5.LED+ DSEN5.LED- DSEN5.C DSEN5.E J,DB37F,DSENSE
J4G DSEN6.LED+ DSEN6.LED- DSEN6.C DSEN6.E J,DB37F,DSENSE
J4H DSEN7.LED+ DSEN7.LED- DSEN7.C DSEN7.E J,DB37F,DSENSE
J4I DSEN8.LED+ DSEN8.LED- DSEN8.C DSEN8.E NC CASE CASE J,DB37F,DSENSE

+5V.I
+5V

CHASSIS C2 10N C73 1N C3 10N C74 1N
CHASSIS C4 10N C75 1N C5 10N C76 1N
CHASSIS C6 10N C77 1N C7 10N C78 1N
CHASSIS C8 10N C79 1N C9 10N C80 1N
CHASSIS C10 10N C81 1N C11 10N C82 1N
CHASSIS C12 10N C83 1N C13 10N C84 1N
CHASSIS C14 10N C85 1N C15 10N C86 1N
CHASSIS C16 10N C87 1N C17 10N C88 1N
CHASSIS C18 10N C89 1N C19 10N C90 1N

RN1A RN,100K
RN1B RN,100K
RN1C RN,100K
RN1D RN,100K
RN4A RN,100K
RN4B RN,100K
RN4C RN,100K
RN7A RN,100K
RN7B RN,100K
RN4D RN,100K

Part C and D of R1402 on page 15

R23 220R
R22 220R
R24 220R
R25 220R
R26 220R
R27 220R
R28 220R
R29 220R
R30 220R

GND

RN2A RN,100K
RN2B RN,100K
RN2C RN,100K
RN2D RN,100K
RN3A RN,100K
RN3B RN,100K
RN3C RN,100K
RN3D RN,100K
RN5A RN,100K
RN5B RN,100K
RN5C RN,100K
RN5D RN,100K
RN6A RN,100K
RN6B RN,100K
RN8A RN,100K
RN8B RN,100K
RN8C RN,100K
RN8D RN,100K
RN6C RN,100K
RN6D RN,100K

U7A U7B U7C U7D U7E U7F
74HC14,SOIC14
U8A U8B U8C
74HC14,SOIC14

Part D, E and F of U1403 on page 15

U5A U6A
CP PL/ CE/ DS D0 D1 D2 D3 D4 D5 D6 D7 Q7 Q7/
IC,74HCT165,SOIC16

GND

SPLIN6 [3]

U5G
AL28 DSEN05.SENSE
AH25 DSEN06.SENSE
AK26 DSEN07.SENSE
AL26 DSEN08.SENSE
XCV300

[18] PD.DSEN18
[18] PD.DSEN19

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Turbo Master Control Electronics
Generic Digital Sensors 1
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DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	R. TOUTANT	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	FEB. 23, 2000	14 of 29

DIGITAL SENSORS FOR ENDPLATE

[3] SPI.SCK7
[3] SPI.PL7/
[3] SPI.CS7/

J6A: DSEN9.LED+, DSEN9.LED-, DSEN9.C, DSEN9.E — J,DB37M,DSENSE
J6B: DSEN10.LED+, DSEN10.LED-, DSEN10.C, DSEN10.E — J,DB37M,DSENSE
J6C: DSEN11.LED+, DSEN11.LED-, DSEN11.C, DSEN11.E — J,DB37M,DSENSE
J6D: DSEN12.LED+, DSEN12.LED-, DSEN12.C, DSEN12.E — J,DB37M,DSENSE
J6E: DSEN13.LED+, DSEN13.LED-, DSEN13.C, DSEN13.E — J,DB37M,DSENSE
J6F: DSEN14.LED+, DSEN14.LED-, DSEN14.C, DSEN14.E — J,DB37M,DSENSE
J6G: DSEN15.LED+, DSEN15.LED-, DSEN15.C, DSEN15.E — J,DB37M,DSENSE
J6H: DSEN16.LED+, DSEN16.LED-, DSEN16.C, DSEN16.E — J,DB37M,DSENSE
J6I: DSEN17.LED+, DSEN17.LED-, DSEN17.C, DSEN17.E, NC, CASE, CASE — J,DB37M,DSENSE

+5V.I, +5V

CHASSIS C49 10N C120 1N C48 10N C119 1N
CHASSIS C47 10N C118 1N C46 10N C117 1N
CHASSIS C45 10N C116 1N C44 10N C115 1N
CHASSIS C43 10N C114 1N C42 10N C113 1N
CHASSIS C41 10N C112 1N C40 10N C111 1N
CHASSIS C39 10N C110 1N C38 10N C109 1N
CHASSIS C37 10N C108 1N C36 10N C107 1N
CHASSIS C35 10N C106 1N C34 10N C105 1N
CHASSIS C33 10N C104 1N C32 10N C103 1N CHASSIS GND

RN16A RN,100K
RN16B RN,100K
RN16C RN,100K
RN16D RN,100K
RN15A RN,100K
RN15B RN,100K
RN15C RN,100K
RN7C RN,100K
RN7D RN,100K
RN15D RN,100K

RN18A RN,100K
RN18B RN,100K — U12A 74HC14,SOIC14
RN18C RN,100K
RN18D RN,100K — U12B 74HC14,SOIC14
RN17A RN,100K
RN17B RN,100K — U12C 74HC14,SOIC14
RN17C RN,100K
RN17D RN,100K — U12D 74HC14,SOIC14
RN14A RN,100K
RN14B RN,100K — U12E 74HC14,SOIC14
RN14C RN,100K
RN14D RN,100K — U12F 74HC14,SOIC14
RN13A RN,100K
RN13B RN,100K — U8D 74HC14,SOIC14
RN12A RN,100K
RN12B RN,100K — U8E 74HC14,SOIC14
RN12C RN,100K
RN12D RN,100K — U8F 74HC14,SOIC14
RN13C RN,100K
RN13D RN,100K

R42 220R, R41 220R, R40 220R, R39 220R, R68 220R, R67 220R, R38 220R, R36 220R, R37 220R — GND

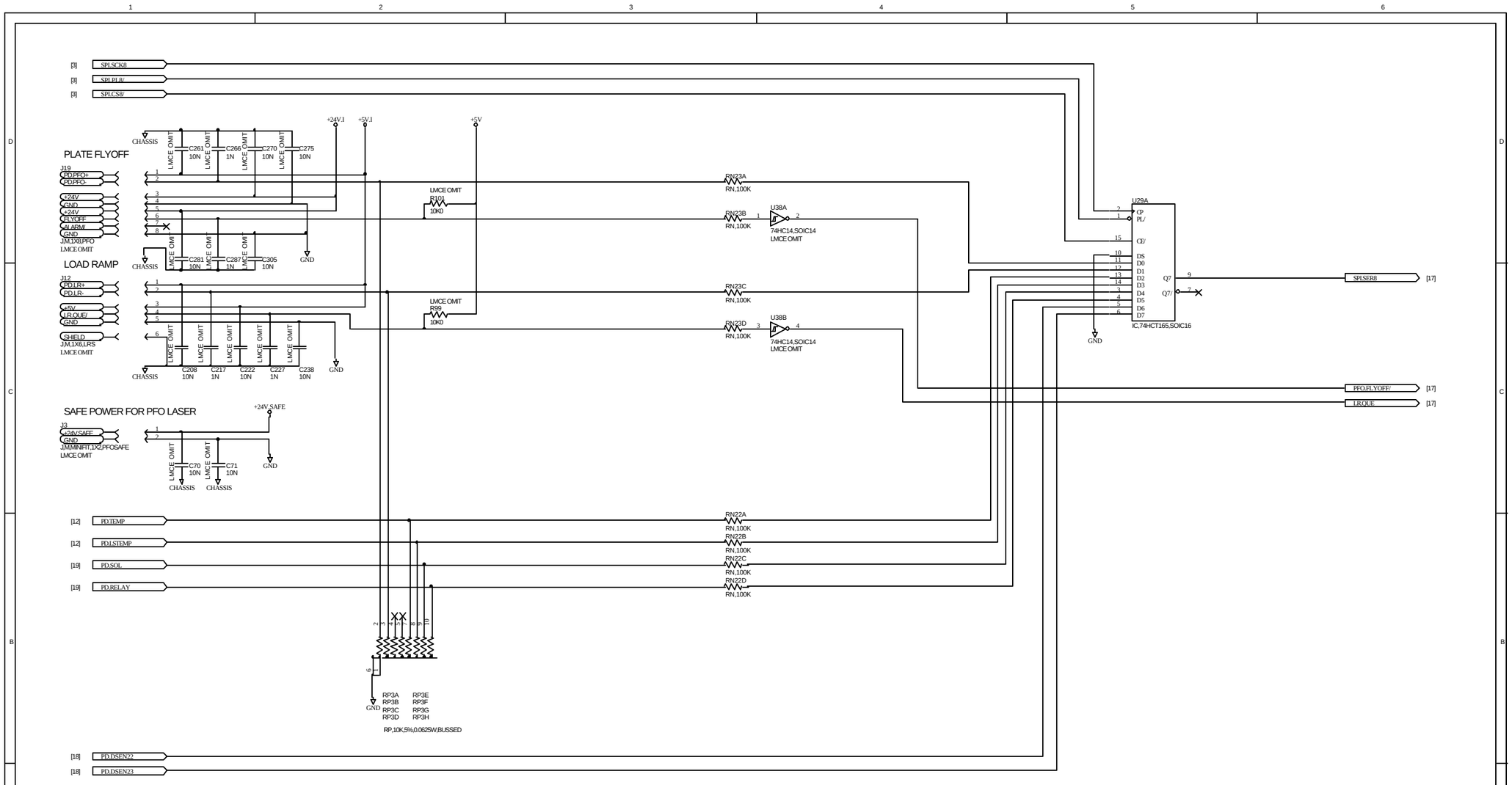
U13A: CP, PL/, CE/, DS, D0, D1, D2, D3, D4, D5, D6, D7, Q7, Q7/ — IC,74HCT165,SOIC16 — GND
U11A: CP, PL/, CE/, DS, D0, D1, D2, D3, D4, D5, D6, D7, Q7, Q7/ — IC,74HCT165,SOIC16
SPI.IN7 [15]

U53H: AJ25 DSEN14.SENSE, AK25 DSEN15.SENSE, AJ24 DSEN16.SENSE, AH23 DSEN17.SENSE — XCV300

[18] PD.DSEN20
[18] PD.DSEN21

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Generic Digital Sensors 2
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\DSENSE2.SCH

DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	R. TOUTANT	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
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Turbo Master Control Electronics

Specific Digital Sensors

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R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	October 25, 2002	16 of 29

[3] SPI.SCK8
[3] SPI.PL8/
[3] SPI.CS8/
[16] SPI.SER8
[19] PD.UINT
[19] UINT.BUT

RN25A RN,100K
RN25B RN,100K
RN25C RN,100K
RN25D RN,100K

U34A
IC,74HCT165,SOIC16
CP
PL/
CE/
DS
D0
D1
D2
D3
D4
D5
D6
D7
Q7
Q7/
SPI.IN8 [3]

+24V.I low voltage detect
Vtrip = 19.2V to 20.8V
+12V.I low voltage detect
Vtrip = 9.56V to 10.3V
+5V.I low voltage detect
Vtrip = 3.84V to 4.10V
-12V.I low voltage detect
Vtrip = -9.54V to -10.5V

+24V.I
R122 45K3
R121 4K99
GND
R120 4K99
+5V
R141 100K
U39A
LM339,SO14N
R142 10KΩ
+5V

+12V.I
R140 20KΩ
R119 4K99
GND
R127 100K
U39B
LM339,SO14N
R133 10KΩ
+5V

+5V.I
R145 10KΩ
R129 10KΩ
GND
R143 100K
U39C
LM339,SO14N
R144 10KΩ
+5V

+5V
R153 4K99
R152 20KΩ
-12V.I
R151 3K32
GND
R128 100K
U39D
LM339,SO14N
R134 10KΩ
+5V

ELECTRONIC REGISTRATION
J21A
+24V
+24V
EREG.PD+
EREG.PD-
GND
GND
JM,2X7,EREG
LMCE OMIT
+24V.I
+5V.I
R102 1K5 LMCE OMIT
LMCE OMIT
C291 10N
C290 10N
C299 10N
C298 1N
C335 10N
C334 10N
CHASSIS
GND

ELECTRONIC REGISTRATION
J21B
EREG.SEN0+
EREG.SEN0-
EREG.SEN1+
EREG.SEN1-
EREG.SEN2+
EREG.SEN2-
EREG.SEN3+
EREG.SEN3-
JM,2X7,EREG
LMCE OMIT
C309 10N
C308 1N
C316 10N
C315 1N
C321 10N
C320 1N
C328 10N
C327 1N
CHASSIS
GND
+5V
LMCE OMIT RN24A RN,100K
LMCE OMIT RN24B RN,100K
LMCE OMIT RN24C RN,100K
LMCE OMIT RN24D RN,100K
RP6A RP6B RP6C RP6D
RP6E RP6F RP6G RP6H
RP,10K,5%,0.0625W,BUSSED

RN26A RN,100K LMCE OMIT
RN26B RN,100K LMCE OMIT
RN26C RN,100K LMCE OMIT
RN26D RN,100K LMCE OMIT
U38C
U38D
U38E
U38F
74HC14,SOIC14
LMCE OMIT

XILINX FPGA (LCA)
U53I
AD31 EREG0
AD30 EREG1
AD29 EREG2
AD28 EREG3
V28 FLYOFF
AA30 LRQUE
XCV300

[16] PCI.FLYOFF/
[16] LRQUE

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Turbo Master Control Electronics
Electronic Registration I/F
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\DSENSE4.SCH

DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	October 23, 2002	17 of 29

Note:
DSENS[18..21] use 1K pullups.

EXTRA DIGITAL SENSORS

+3V1 +5V

J5A
DSEN18.LED
DSEN18.LED
DSEN18.C
DSEN18.E
J.DB25F.DSENSE
*
J5B
DSEN19.LED
DSEN19.LED
DSEN19.C
DSEN19.E
J.DB25F.DSENSE
LMCE OMIT
J5C
DSEN20.LED
DSEN20.LED
DSEN20.C
DSEN20.E
J.DB25F.DSENSE
LMCE OMIT
J5D
DSEN21.LED
DSEN21.LED
DSEN21.C
DSEN21.E
J.DB25F.DSENSE
LMCE OMIT
J5E
DSEN22.LED
DSEN22.LED
DSEN22.C
DSEN22.E
J.DB25F.DSENSE
LMCE OMIT
J5F
DSEN23.LED
DSEN23.LED
DSEN23.C
DSEN23.E
NC
CASE
CASE
J.DB25F.DSENSE
LMCE OMIT

LMCE OMIT
C20 10N, C91 1N, C21 10N, C92 1N → CHASSIS
C22 10N, C93 1N, C23 10N, C94 1N → CHASSIS
C24 10N, C95 1N, C25 10N, C96 1N → CHASSIS
C26 10N, C97 1N, C27 10N, C98 1N → CHASSIS
C28 10N, C99 1N, C29 10N, C100 1N → CHASSIS
C30 10N, C101 1N, C31 10N, C102 1N → CHASSIS
CHASSIS

RN10A RN,100K
RN10B RN,100K
RN10C RN,100K
RN10D RN,100K
RN11A RN,100K
RN11B RN,100K
RN11C RN,100K LMCE OMIT
RN11D RN,100K LMCE OMIT

R31 220R, R32 220R, R34 220R, R33 220R, R65 220R, R66 220R → GND

RN9A RN,100K
RN9B RN,100K
RN9C RN,100K
RN9D RN,100K
RN19A RN,100K
RN19B RN,100K
RN19C RN,100K
RN19D RN,100K
RN20A RN,100K
RN20B RN,100K
RN20C RN,100K
RN20D RN,100K

U9A 74HC14,SOIC14 LMCE OMIT
U9B 74HC14,SOIC14 LMCE OMIT
U9C 74HC14,SOIC14 LMCE OMIT
U9D 74HC14,SOIC14 LMCE OMIT
U9E 74HC14,SOIC14 LMCE OMIT
U9F 74HC14,SOIC14 LMCE OMIT

PD.DSEN18 [14]
PD.DSEN19 [14]
PD.DSEN20 [15]
PD.DSEN21 [15]
PD.DSEN22 [16]
PD.DSEN23 [16]

U53J XCV300
AA29 DSEN18.SENSE
AB31 DSEN19.SENSE
AB29 DSEN20.SENSE
AB28 DSEN21.SENSE
AC30 DSEN22.SENSE
AC29 DSEN23.SENSE

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Extra Generic Digital Sensors
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DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
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The 470R resistors limits the current to the TPIC drivers (safety requirement).
They should be placed as close as possible to the TPIC drivers.

The MCE can detect whether the solenoids are connected by using a loop-back on pins 2 and 4.

SOLENOID / RELAY DRIVERS

U2A, U17A, U27A — TPIC6595

SER IN, RCK, SRCK, G (ENABLE), SRCLR, DRAIN0–DRAIN7, SER OUT

+5V: R17 2K7 (SPI.MOSI [2], SPI.CS4/ [3], SPI.SCK4 [3], DRV.EN/ [2])
R5, R4, R16, R15, R21, R20, R56, R54, R64, R62 — 470R

+5V: R98 2K7 (SPI.CS5/ [3], SPI.SCK5 [3])

+5V.I: R61, R63, R53, R55 — 470R (PD.SOL [16])

C141, C143, C145, C144, C147, C146, C152, C151, C140, C142 — 1N (CHASSIS)

C158, C157, C161, C167, C185, C187, C191, C194 — 1N (CHASSIS)

C383, C384, C401, C402, C415 — 10N; C416 — 1N (CHASSIS)

C242, C241, C246, C245, C248 — 1N (CHASSIS)

R96 1K00 (+5V)

SOLENOID DRIVERS

J10B — JM,2X13,SOLENOID

DRV0S/D, DRV1S/D, DRV2S/D, DRV3S/D, DRV4S/D, DRV5S/D, DRV6S/D, DRV7S/D, DRV8S/D, DRV9S/D, DRV10S/D, DRV11S/D

+24V.SAFE

RELAY DRIVERS

J24B — JM,MINIFIT,2X4,RELAY

RELAY0+/0-, RELAY1+/1-, RELAY2+/2-

+24V.I

USER INTERFACE

J16B — JM,2X5,UI LMCE OMIT

UINT.LED0, UINT.LED1, UINT.LED2, UINT.LED3, UINT.BUZ

LMCE ONLY

J48A — JM,MINIFIT,2X3,SOL TMCE OMIT

DRV0S, DRV1S, DRV2S, DRV3S — SOL1, SOL2, SOL3, SOL4

J48B — JM,MINIFIT,2X3,SOL TMCE OMIT

NC, NC

SOLENOID DRIVERS

J10A — JM,2X13,SOLENOID

+24V, +24V — +24V.SAFE

C201 10N, C200 10N (CHASSIS)

RELAY DRIVERS

J24A — JM,MINIFIT,2X4,RELAY

PD.RELAY+, PD.RELAY-

+5V.I

C365 10N, C366 1N (CHASSIS)

USER INTERFACE

J16A — JM,2X5,UI LMCE OMIT

UINT.+24V, UINT.+24V

UINT.BUT, UINT.PD, UINT.+5V

+24V.I, +5V.I

C228 10N, C229 10N, C247 1N, C257 1N, C256 10N (CHASSIS)

PD.RELAY [16], UINT.BUT [17], PD.UINT [17]

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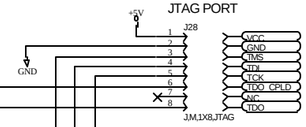
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Solenoid Driver and User Interface

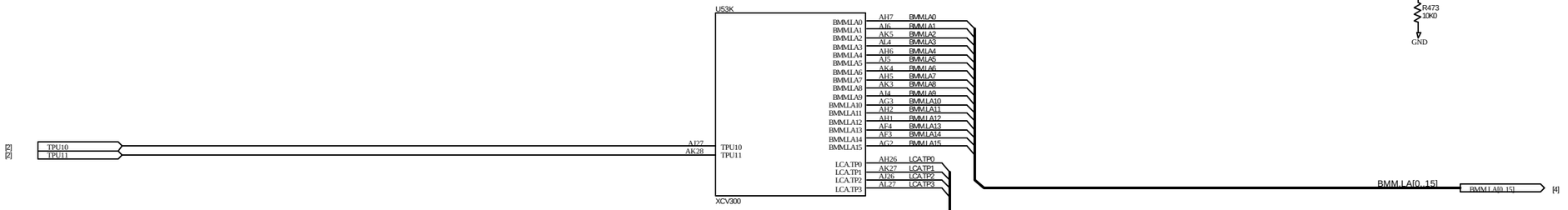
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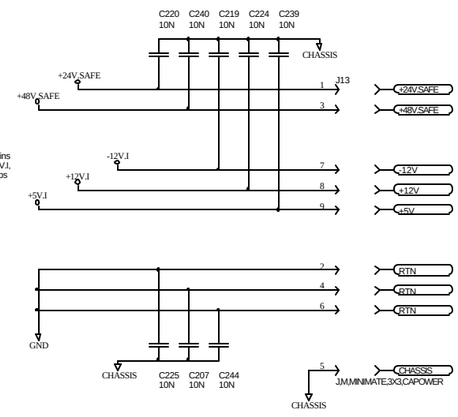
JTAG PORT



XILINX FPGA (LCA)

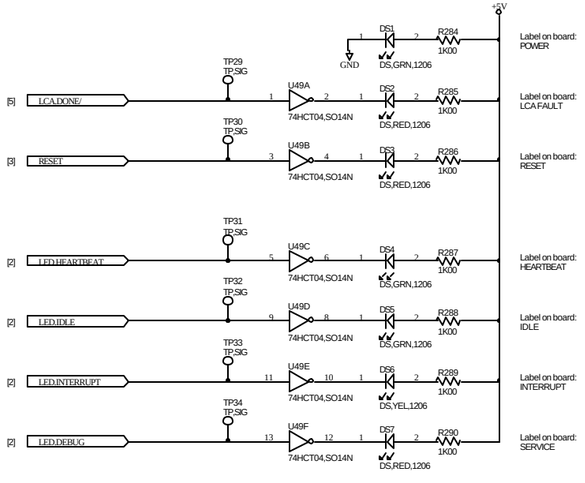


CARRIAGE AMP POWER CONNECTOR

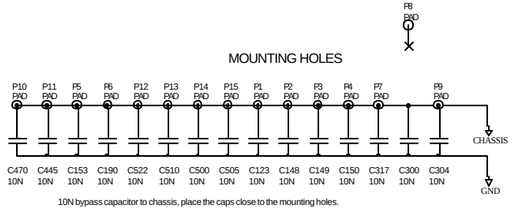


Make sure all the pins are supplied with big fat traces. Also, put at least one 22U decoupling cap close to the pins of the connector, on +5V.I, +12V.I, and -12V.I lines. (at least 3 caps total)

STATUS LEDS

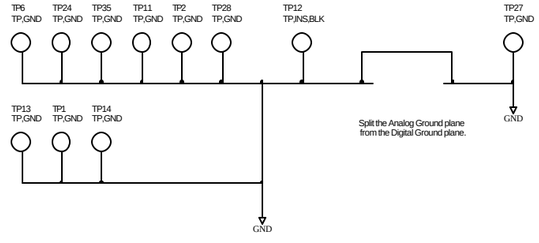


MOUNTING HOLES



10N bypass capacitor to chassis, place the caps close to the mounting holes.

GENERAL GROUND TEST POINTS



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EXPANSION BUS (SCON)

J9A
+48SAFE
+48SAFERTN
+24SAFE
+24SAFERTN
+24V
+24VRTN
J,M,MINIFIT,2X5,EXPBUS

EXPANSION BUS (SCON)

J7A
+48SAFE
+48SAFERTN
+24SAFE
+24SAFERTN
+24V
+24VRTN
CHASSIS
J,M,MINIFITJR,2X8

**** IMPORTANT NOTE ABOUT J7 ****
On 10-4766D-C, we have elected to leave a 16 pin footprint, but populated it with a 10 pin MiniFit Jr header. This means that the part number generated by Protel will be incorrect, even though this problem has been dealt with in Agile. This means that some of the pin numbers in the schematic don't match the physical pin numbers on the 10-pin header.

With this in mind, please find the appropriate pin number correlation table below.

Schematic (footprint) pin # — 10-pin physical pin #

1 — 1
2 — 2
2 — 2
3 — 3

+48V.SAFE
D4 D,MBRS360
C184 10N
C156 10N
CHASSIS
GND

+24V.SAFE
D3 D,MBRS360
C183 10N
C155 10N
CHASSIS
GND

+24V
D2 D,MBRS360
C182 10N
C154 10N
CHASSIS
GND

R173 1M00
C560 100N
CHASSIS

+5V
R86 10KO
R80 2K7
U18
R85 100K
SFH6156-3
+24V.SAFE_ON/ [2]
GND

FIRMWARE DETECT SAFETY STATUS

+5V
R91 10KO
R88 2K7
R89 2K7
U24
R90 100K
SFH6156-3
+48V.SAFE_ON/ [2]
GND

+5V
R219 1K00
C355 10N
CHASSIS

J7C
BRD_LOC+
BRD_LOC+
BRD_LOCD-
BRD_LOC1-
BRD_LOC2-
BRD_LOC3-
J,M,MINIFITJR,2X8

[2] TPU12 — R209 100K — R224 10KO — R230 10KO — R231 10KO — R232 10KO — GND
[2] TPU13 — R216 100K
[2] TPU14 — R217 100K — C360 10N — C364 10N — C558 10N — C559 10N — CHASSIS
[2] TPU15 — R218 100K

CAN TRANSCEIVER

[2] CAN.TXD
U1A
TXD RXD
CANH
CANL
RS VREF
PCA82C250,SO8
CAN.RXD [2]
GND

Place the CAN transceiver very close to the inside edge of the metal can.
The CANH and CANL lines cannot be decoupled because of capacitance problems.

EXPANSION BUS (SCON)

J8B
CAN_H
CAN_L
J,M,MINIFIT,2X5,EXPBUS

EXPANSION BUS (SCON)

J7D
CAN_H
CAN_L
J,M,MINIFITJR,2X8

C138 OMIT
C139 OMIT
CHASSIS

R2 100K
R1 22K0
C1 1U0
GND
TERMDET [2]

EXPANSION BUS (SCON)

J8C
TERM_DET
CHASSIS
J,M,MINIFIT,2X5,EXPBUS

C72 10N
R3 1M00
CHASSIS
CHASSIS

EXPANSION BUS (SCON)

J7B
TERM_DET
J,M,MINIFITJR,2X8

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Expansion Bus (SCON)
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R. TOUTANT	D. LOWE	
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Use MECH9 and MECH10 to secure U40 (2.5V regulator, TO220) to the PCB.

MECH9 SCRW,M3*6

MECH10 NUT,M3

+5V

U40 LM1117-ADJ VIN VOUT TAB ADJ

C280 22U GND

R94 100R

R95 100R GND

C338 22U GND

C460 22U GND

TP26 TP,INS,RED +2.5V

+2.5V

+24V

F3 F,POLYSWITCH,1.85A,30V,RUE185

FERRITE L4

C192 10N GND

C193 10N GND

TP9 TP,INS,RED +24V

+24V

F2 F,POLYSWITCH,1.85A,30V,RUE185 +24V.I

SWITCHER, +12V

L10 L,0U22,1025MA

C253 220UF GND

C263 100N GND

U35 LM2672M-ADJ SS SYNC FB CB VIN VSW ON/OFF GND

C272 10N GND

R112 22K1

R113 2K49 GND

C284 10N

D8 D,MBRS340 GND

L11 L,150UH,DO3316P-154

L13 OMIT L,150UH,PE-53819

TP15 TP,INS,RED +12V

C252 220UF GND

FERRITE L15

F4 F,POLYSWITCH,0.5A,15V,MINISMDC050

C412 22U GND +12V

C223 22U GND +12V.I

FERRITE L17

C490 22U GND +12V.A

Populate U41, or U35 and the associated circuit in the dotted line (default).

Populate U42, or U36 and the associated circuit in the dotted line (default).

Populate U19, or U28 and the associated circuit in the dotted line (default).

U41 OMIT PT5102N VIN VOUT GND

Populate L11 or L13
Populate L12 or L14
Populate L6 or L5
Populate D6 or D5

SWITCHER, -12V

U36 LM2672M-ADJ SS SYNC FB CB VIN VSW ON/OFF GND

C273 10N

R114 22K1

R115 2K49

C285 10N

D7 D,MBRS340

56UF,50V,ELEC C265

C278 100N

D9 D,MBRS340

L12 L,150UH,DO3316P-154

L14 OMIT L,150UH,PE-53819 GND

TP16 TP,INS,RED -12V

C254 220UF GND

C491 22U GND -12V

FERRITE L19

C486 22U GND -12V.A

FERRITE L16

F5 F,POLYSWITCH,0.5A,15V,MINISMDC050

C218 22U GND -12V.I

L7 L,0U22,1025MA

C255 220UF GND

C264 100N GND

U42 OMIT PT78NR112V VIN VOUT GND

C397 22U GND

C188 22U GND

C212 22U GND

C331 22U GND +5V

FERRITE L18

C442 22U GND +5V.A

TP9 TP,INS,RED +24V

+24V

FERRITE L4

F3 F,POLYSWITCH,1.85A,30V,RUE185

C192 10N GND

C193 10N GND

SWITCHER, +5V

The collection of 9 omitted 5V supply components that were here in the TMCE 10-4766C-A and LMCE 10-4949A-A have been deleted. (C210,C243,D5,L5,L6,R97,R110,R100,U28) -Dean Lowe October 24, 2002

L9 L,0U15,2450MA

C234 220UF GND

C233 220UF GND

C232 220UF GND

C211 100N GND

U19 PT6653P VIN VIN VIN VOUT VOUT VOUT STBY GND GND GND GND RSENSE

TP10 TP,INS,RED +5V

C231 220UF GND

C209 220UF GND

FERRITE L8

F1 F,POLYSWITCH,1.85A,30V,RUE185

C164 22U GND +5V.I

REGULATOR, +3.3V

U63 LT1529-3.3,DD5 IN OUT SHDN SENS GND GND

C312 22U GND

C396 22U GND

C461 22U GND

C381 22U GND

TP25 TP,INS,RED +3.3V

+3.3V

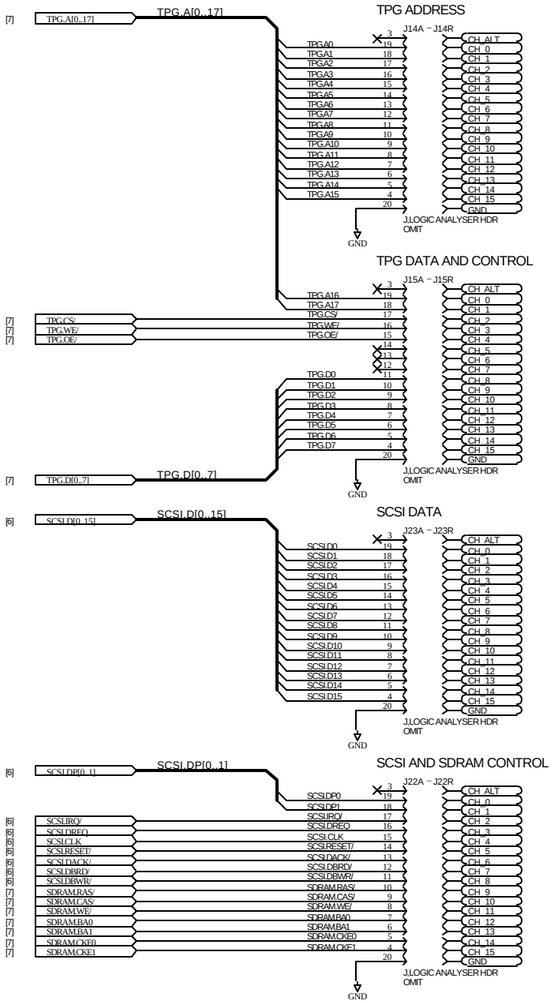
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Power Supplies

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ANDREW C.L. LAU	D. LOWE	
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Logic Analyzer Headers

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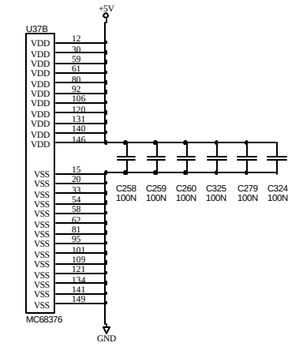
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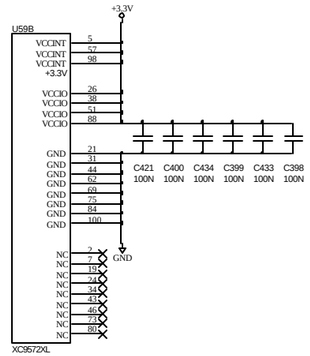
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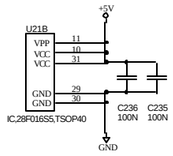
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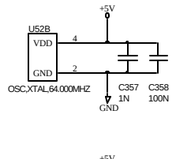
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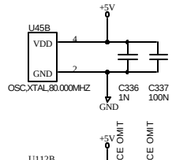
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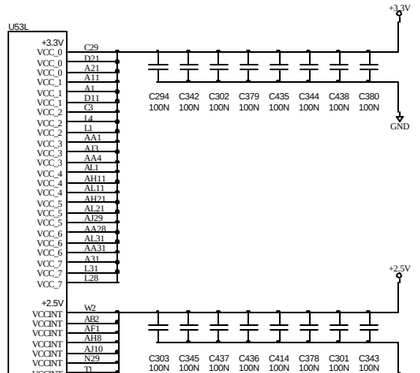


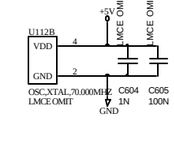


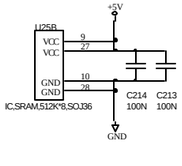


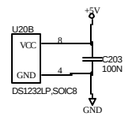


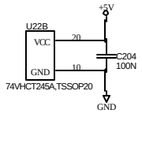


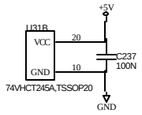


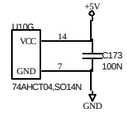


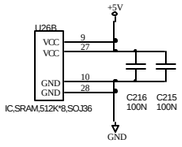


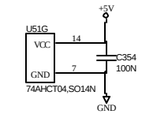


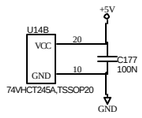


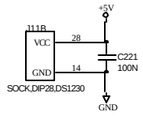


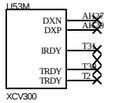












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Power Sheets 2 to 5

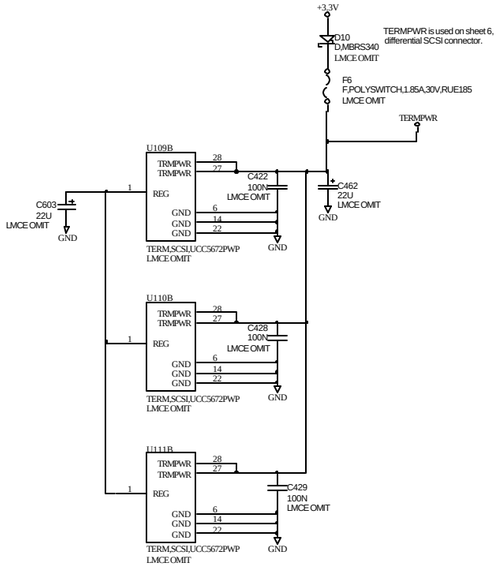
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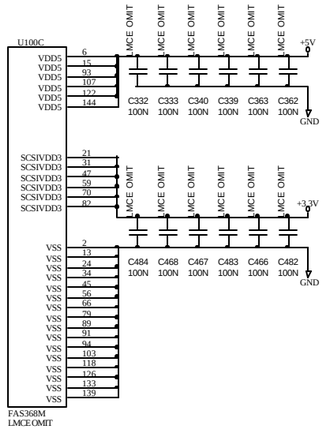
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R. TOUTANT	713-04766D-C	CA00911
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
R. TOUTANT	D. LOWE	
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
1999:08:23	October 25, 2002	24 of 29

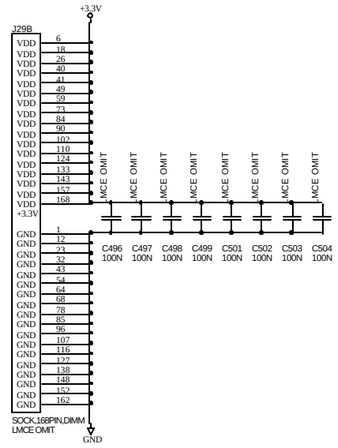
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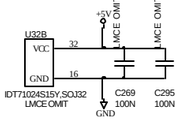
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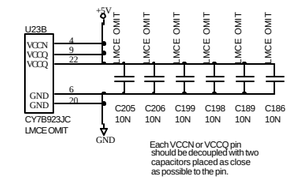
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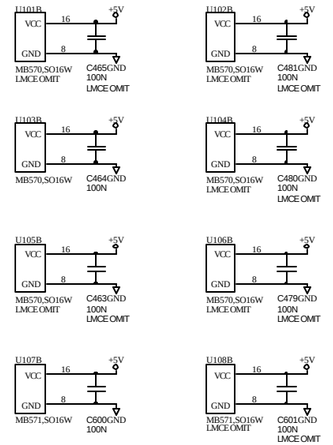












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DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 26, 2002	SHEET: 25 of 29

SHEET 8

SHEET 9

SHEET 10

SHEET 11

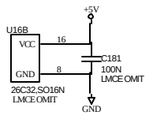
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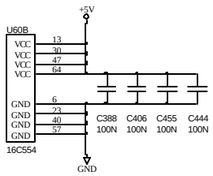
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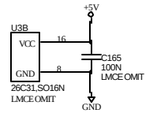
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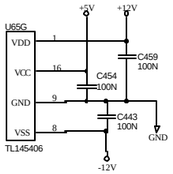
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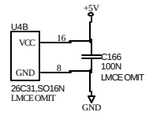
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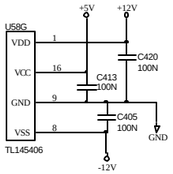


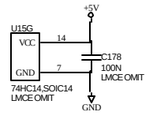


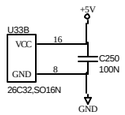


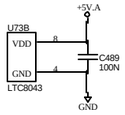


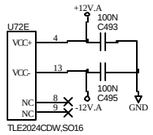


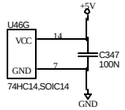


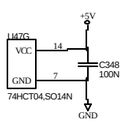


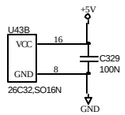


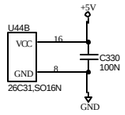


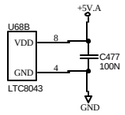


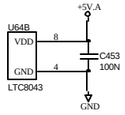


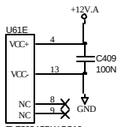


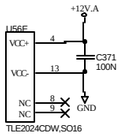


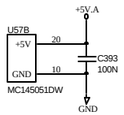


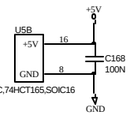


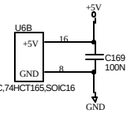


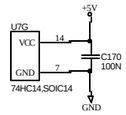


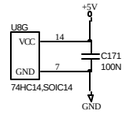


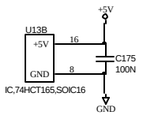


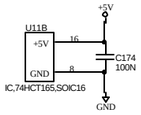


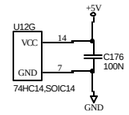


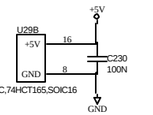


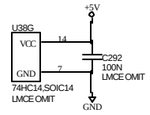


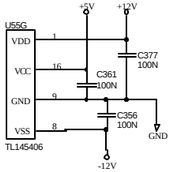


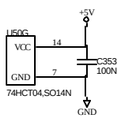












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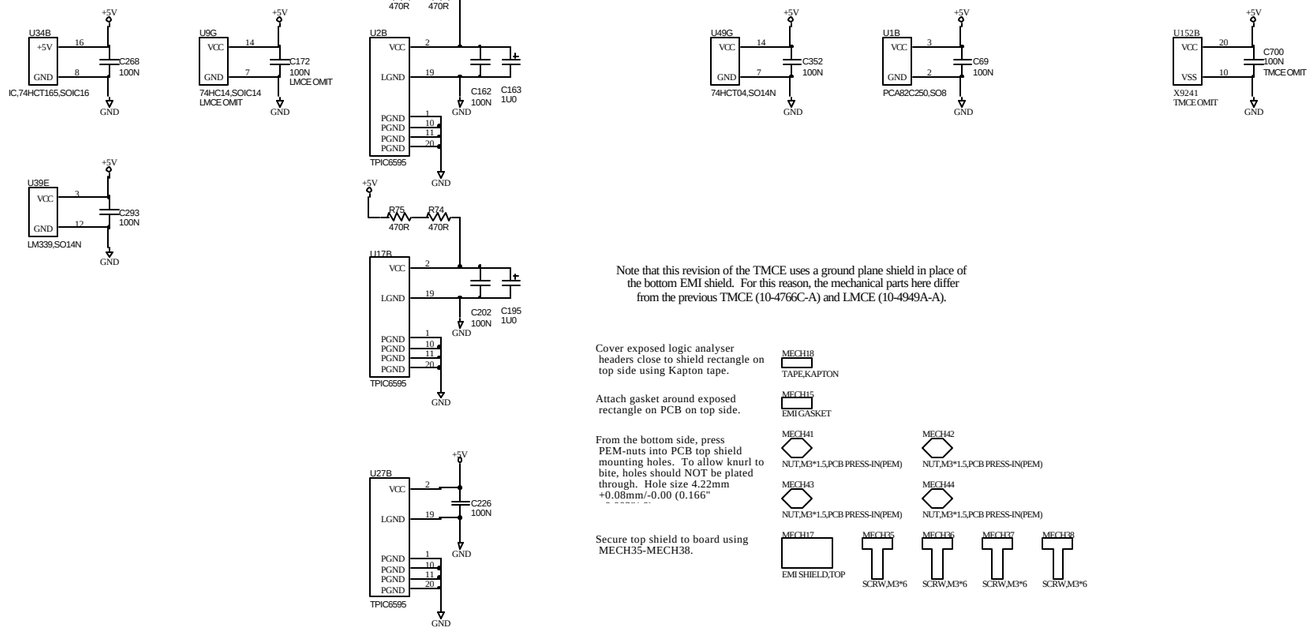
Turbo Master Control Electronics

Power Sheets 8 to 16

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DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 23, 2002	SHEET: 26 of 29

SHEET 17 | SHEET 18 | SHEET 19 | SHEET 20 | SHEET 21 | SHEET 29



Note that this revision of the TMCE uses a ground plane shield in place of the bottom EMI shield. For this reason, the mechanical parts here differ from the previous TMCE (10-4766C-A) and LMCE (10-4949A-A).

Cover exposed logic analyser headers close to shield rectangle on top side using Kapton tape.

MECH18
TAPE,KAPTON

Attach gasket around exposed rectangle on PCB on top side.

MECH15
EMI GASKET

From the bottom side, press PEM-nuts into PCB top shield mounting holes. To allow knurl to bite, holes should NOT be plated through. Hole size 4.22mm +0.08mm/-0.00 (0.166"

MECH41
NUT,M3*1.5,PCB PRESS-IN(PEM)
MECH42
NUT,M3*1.5,PCB PRESS-IN(PEM)
MECH43
NUT,M3*1.5,PCB PRESS-IN(PEM)
MECH44
NUT,M3*1.5,PCB PRESS-IN(PEM)

Secure top shield to board using MECH35-MECH38.

MECH17
EMI SHIELD,TOP
MECH35
SCRW,M3*6
MECH36
SCRW,M3*6
MECH37
SCRW,M3*6
MECH38
SCRW,M3*6

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Turbo Master Control Electronics

Power Sheets 17 to 21

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DESIGNED BY: R. TOUTANT	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: R. TOUTANT	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: 1999:08:23	LAST MODIFIED DATE: October 23, 2002	SHEET: 27 of 29

Route all "PE_" traces as follows:

- Differential signals should be 6 mils wide, with 6 mils separation for as long as possible (eg. PE_NSP1_11+ should be 6 mils wide, and separated from PE_NSP1_11- by 6 mils).
- All other adjacent tracks should be at least 12 mils apart (eg. PE_NSP1_11+ should be at least 12 mils from everything else but PE_NSP1_11-).
- Equalize differential pair net lengths to within 50 mils (eg. PE_NSP1_11+ and PE_NSP1_11- net lengths should equal each other to within 50 mils).
- Equalize all "PE_NSP1*" net lengths to within 500 mils.
- Equalize all "PE_NSP2*" net lengths to within 500 mils.

Place series resistors as close to source as possible.

Place these series resistors as close to source as possible.

"NSP1*" and "NSP2*" routing:

Equalize all "NSP1*" net lengths to within 500 mils (except for NSP1_OE/).
Equalize all "NSP2*" net lengths to within 500 mils (except for NSP2_OE/).

Place 100R resistors as close to the input pins on the MB570 as possible.

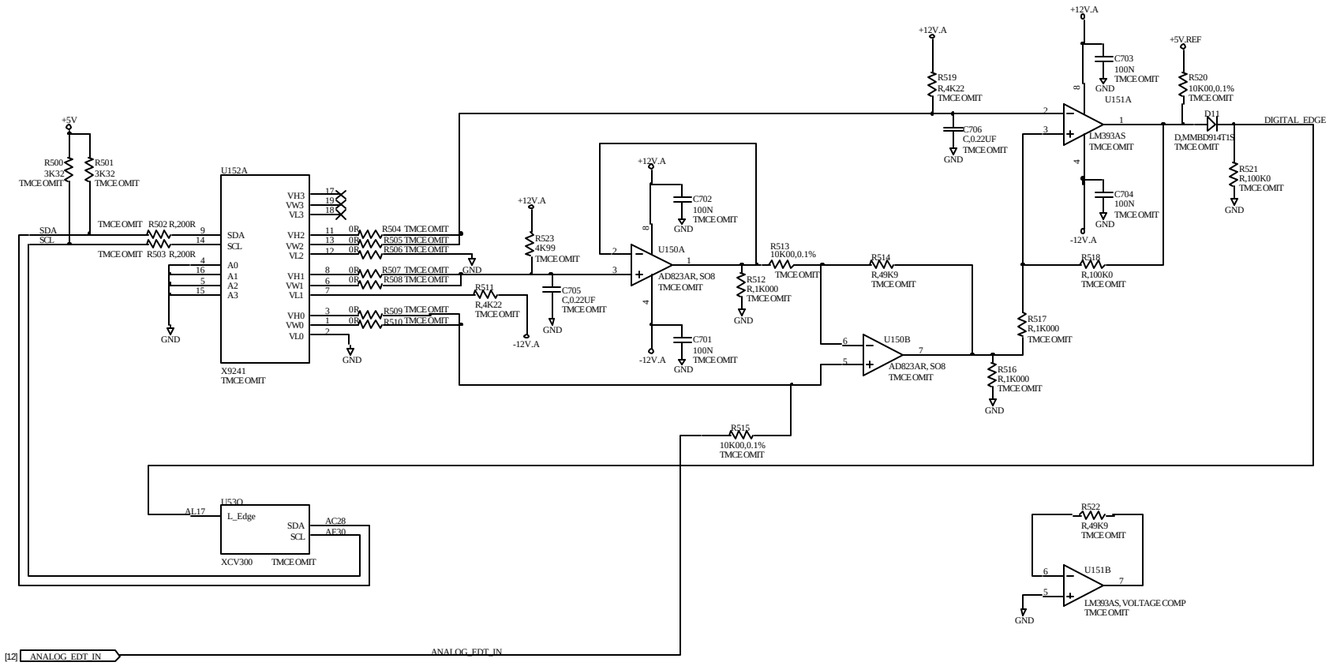
Attach spacers (aka jack screws), nuts, and lock washers into mounting holes of

LIF INTERFACE

DESIGNED BY: J.MALM	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: CA00911
DRAWN BY: J.MALM	LAST REVISED BY: D.LOWE	APPROVED BY:
DESIGN DATE: 2000:06:26	LAST MODIFIED DATE: January 15, 2003	SHEET: 28 of 29

Turbo Master Control Electronics
Turboscreening Interface
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This sheet contains components that are unique to the LMCE ONLY. Therefore, they are all TMCE OMIT.



creo	Lotem Master Control Electronics	
	Analog Edge Detect	
C:\My Documents\Desktop\TurboMce version D-C.ddb - Documents\EDGE.SCH		
DESIGNED BY: L. SCHWARTZ	DOCUMENT NUMBER: 713-04766D-C	LAST ECO: ???
DRAWN BY: L. SCHWARTZ	LAST REVISED BY: D. LOWE	APPROVED BY:
DESIGN DATE: March 22, 2001	LAST MODIFIED DATE: October 26, 2002	SHEET: 29 of 29