Theory of Operations (Draft)

MCE	Master Control Electronics
PDB	Power Distribution Board
GENINE	GENeric Input/output Node Electronics

MCE

The TURBOMCE board contains all the control and imaging electronics to control a base Trendsetter machine. It does not include the Spectrum or Autoloader options, but does support the upgrade/expansion to these options with satellite boards (GENINE).

The TURBOMCE board replaces:

- MPE
- ALE
- FDPE
- Card cage/backplane
- 1/3 TEE

The MCE uses code from the new FW1 (Firmware 1) environment.

MCE - Microcontroller and Firmware Functions

- Download and update new firmware via a serial link to the workstation.
- Download boot block recovery firmware with the Bootstrap Memory Module.
- Automatically boot up, perform self-check, and initialize the on board FPGA.
- Store state variables and non-volatile parameters.

Microcontroller Unit

The Motorola MC68376 Microcontroller is a 32 bit microcontroller

- that runs 68000 code on a multithreaded kernel
- has a 24 bit address bus that can address 16 Mbytes of memory
- has an integrated CAN bus controller for satellite board expansion
- has a serial interface to diagnostics computer/laptop, and to on-board SPI components

The MCU contains a QSM (Queued Serial Module) for downloading firmware through the RS-232 Diagnostic Interface to PC. The highest baud rate that can be generated reliably by the MCU is **57.6 kBaud**, with less than 1.4% error. In the future, the diagnostics interface and the workstation interface might be combined into one unified interface. This would eliminate having two RS-232 serial cables from the workstation to the CTP.

A built-in Queued SPI bus is used locally on the MCE board to interface to slow peripherals such as solenoid drivers, DAC's and A/D's that do not need a high-speed parallel bus. The SPI bus reduces pin count and cost.

Memory

Flash (Code)

The MCE has two 2Mx8 symmetric-blocked Flash memory chips. These chips are single voltage, 5V CMOS parts.

The first sector or block of Flash is write protected by the logic in the CPLD. The chip select line of the Flash is simply disabled if the processor tries to write to the first block of memory, unless the BMM card is plugged in. This method of protection allows the use of non-boot-block type of memory, yet affords the same level of protection as boot-block memory. It also allows greater flexibility, as the number of sectors to be protected is variable.

SRAM (Data) Memory

The MCU incorporates two 512Kx8 SRAM memory chips in 400mil 36-pin SOJ package.

NVRAM

The MCE uses one 32kx8 battery-backed NVRAM module in a 28 pin 600mil DIP package.

Bootstrap Memory Module (BMM)

A Bootstrap Memory Module (BMM) is provided to program the boot code of the Flash memory in the system. It uses a 100-pin connector to the MCE board. The BMM has test LEDs to make firmware debugging easier, a Background Debug Port from the MCU, and analyzer headers for all of the bus signals. A jumper can be installed on the BMM to force the microcontroller to execute from the Flash code instead of from the BMM even with the BMM installed.

MCE - Clock Generation

The TURBOMCE board has three crystal oscillators, 64MHz, 70MHz, and 80MHz. All other timing signals are derived from these three oscillators. The raw clock rates are piped into both the CPLD and the PCU, where clocks for the various chips are generated.

Required Frequencies

The following diagram illustrates the various clock rates required by the different chips.

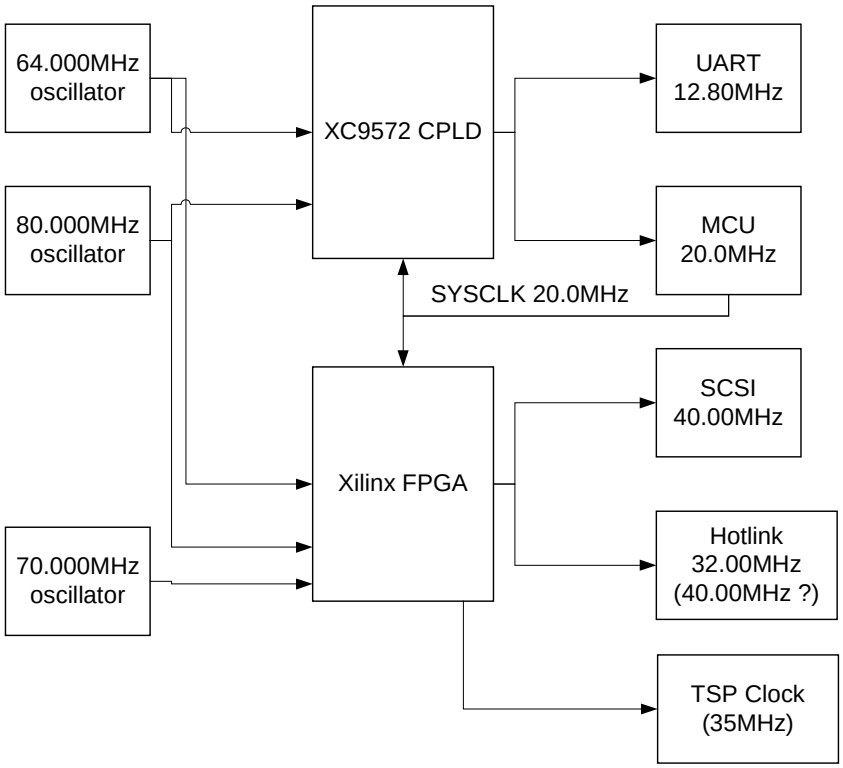


Figure 1: Clock Generation and distribution

The following is a table of the various components that require a clock and where the clock is generated.

Device	Requires	Generate from (OSC)	Divided in	Divisor	Comment
MCU (MC68376)	20.00MHz	80.00MHz	CPLD	4	
UART	12.80MHz	64.00MHz	CPLD	5	
SCSI	40.00MHz	80.00MHz	LCA	2	
Hotlink	32.00MHz	64.00MHz	LCA	2	Can be upgraded to 40.00MHz
TSP	35.00MHz	70.00MHz	LCA	2	Used for Turboscreen Interface

The Hotlink currently requires 32MHz, but may require 40MHz in the future to use with the new thermal heads. The current scheme allows reprogramming of the Xilinx to generate 40MHz from the 80MHz oscillator in the future.

MCE - Imaging Data Path

Input

Ultra SCSI interface

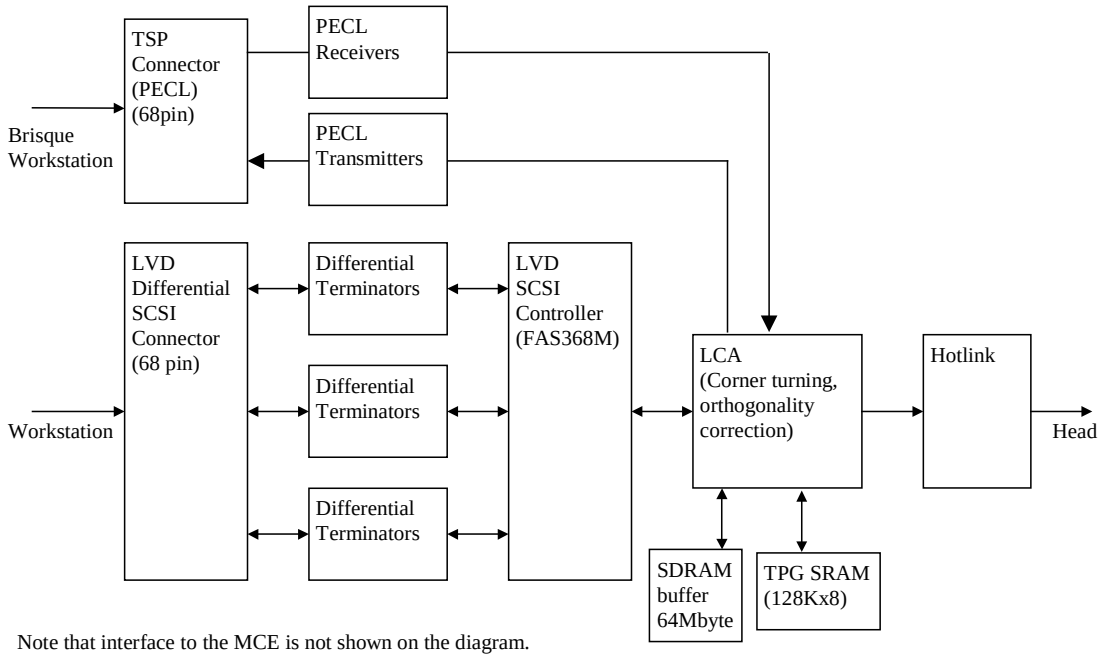
PECL interface to Brisque workstation

Data-path

- **240 Mbit/s throughput**
- **Hardware corner turning and orthogonality correction**
- **Test-pattern generation (TPG)**

Output

Hotlink to Thermal head -



Note that interface to the MCE is not shown on the diagram.

Ultra SCSI Interface (J42)

Data from the RIP transfers to the MCE board over a differential Ultra SCSI bus – see schematic. The Fast Architecture SCSI Controller (FAS368M) is capable of running in Fast mode at 40Mbyte/second, normal mode at 20Mbyte/second, and Fast Wide mode at 80Mbyte/second. It interfaces to the FPGA (data), and the MCU (control). The SCSI uses LVD (Low Voltage Driver) interface. instead of HVD to free up board space for the (PECL) interface circuitry to Brisque. Since we're still using HVD workstations we need an external HVD-LVD converter.

PECL Interface to Brisque Workstation

A secondary data transfer method uses the TSP interface that communicates with TSP boards in a Brisque workstation. The interface consists of thirteen differential PECL signals -- eleven inputs and three outputs. The PECL inputs are converted to TTL levels and are read by the FPGA.

The turboscreening interface runs at clock speeds up to 35MHz. A 70MHz oscillator is added to the board to generate the 35MHz clock.

Cable detect is performed by either the FPGA detecting the presence of a 35MHz clock from the TSP board(s), or a loopback on the connector read by the TSP boards.

Hardware Corner turning and Orthogonality Correction

The FPGA takes raw image data from the SCSI Controller and does 3+ swath data-buffering, corner-turning and orthogonality correction.

Geometric correction is:

Any parallelogram to parallelogram:

- XY scaling
- XY shift
- Rotation
- Skew

Non-linear mainscan shift (track correction)

Drum taper, non-linear mainscan scale

- not currently supported in firmware
- Hardware does support

The LCA also controls the data flow of the SCSI Controller. The FDPE part of the LCA is unmodified from FDPE except for

- the processor-bus interface
- 128k x 8 TPG SRAM instead of 64k x 16 configuration.

Test Pattern Generator (TPG) SRAM

The Test Pattern Generator SRAM, plots a test image generated by the microcontroller without using the SCSI data path. The SRAM is written by the MCU, then used to emulate the data coming from the SCSI port. The TPG has its own address and data bus from the FPGA. The TPG SRAM and interface is slightly different from the previous FDPE. Instead of using 3.3V, 64Kx16 SRAM on the FDPE, the TURBOMCE uses 128kx8 SRAM, so that fewer pins are needed to interface to the TPG SRAM from the Xilinx.

Hotlink to Thermal Head

A Hotlink (ECL) transmitter transfers image data to the thermal head. The Hotlink requires a 32MHz clock that is divided from the 64MHz oscillator. The Hotlink transmitter is interfaced to the LCA in a similar fashion to the one on the FDPE board.

320Mbit/sec Hotlink-based data rate to the head

The Hotlink data bus HLI.D[0..8], HLI.ENA/ and HLI.CLKO are connected to a logical analyzer on the TURBOMCE to enable debugging. The output side of the Hotlink RF transformer is grounded

to CHASSIS ground instead of the regular digital ground to reduce noise. (See schematics for more details). The output side of the second half of the RF transformer is grounded to signal GND to prevent accidental shorting of chassis ground with signal ground when using oscilloscopes with two probes.

MCE - Communications

Serial ports (RS232)

- **Work Station**
- **Diagnostic**
- **Dongle**
- **Plate Processor or Spare**

CAN Bus

JTAG

Onboard Status LEDs

Ultra SSCI – see Image Data Path and Head Interface section

Hotlink and exposure head interface; – see Image Data Path and Head Interface section

Omitted - Background Debug mode header and the logical analyzer headers on the BMM module.

RS-232 Ports

4 serial ports:

- Work Station (J39)
- Diagnostics (J40)
- Dongle (J37)
- Plate Processor or Spare (J38)

All 4 ports are set up as Data Communication devices so that a null modem cable is not required for connection to a standard 9-pin serial port on a computer. A single 16C554 UART chip on the MCE board controls all 4 serial ports. This is simply a quad version of the popular 16C550 found in most PC's.

Pinouts for all ports

Pin	Diagnostic Port	Workstatio Port	Dongle Port	Spare Port
1	Not connected	Not Connected	Not Connected	Not Connected
2	RX	RX	RX	RX
3	TX	TX	TX	TX
4	DTR	Shorted to DSR	DTR	Shorted to DSR
5	Not connected	Not Connected	Not Connected	Not Connected
6	DSR	Shorted to DTR	DSR	Shorted to DTR
7	RTS	Shorted to CTS	RTS	Shorted to CTS
8	CTS	Shorted to RTS	CTS	Shorted to RTS
9	Not connected	Not Connected	Not Connected	Not Connected

The diagnostics port is used to download firmware onto the CTP from a PC laptop or from the workstation. The port also allows remote diagnostics trhough the work station by modem dial-up.The maximum reliable baud rate is 57.6k

CAN (Controller Area Network) Bus

The CAN bus carries communication between the MCE board and the satellite boards. (a Philips 82C250, surface-mount 8-pin CAN transceiver). The CAN signals are carried in the same connector as the main power distribution and safety loop (see table).

J7, J8 (SCON1, SCON2) MINIFIT2X5

Pin	Name	Function	Comment
1	+48SAFE	+48V Safety switched supply	Used to drive carriage amp on the MCE
2	+48SAFERETN		
3	+24SAFE	+24V Safety switched supply	Used to drive solenoids
4	+24SAFERTN		
5	+24V	+24V non-switched supply	Powers DC-DC switching regulators (+5V, +12V, -12V, +3.3V, +2.5V)
10	+24VRTN		
6	CAN_H	CAN differential pair	-
7	CAN_L		
9	TERM_DET	Termination detect	When both terminators are properly attached, the TERM_DET line should read about +12V. (0V or +24V otherwise)
8	CHASSIS	Shielding connection	-

JTAG Port

- For programming the onboard Xilinx
- For development use only

Status LEDs

Seven LEDs on the board visually indicate the status of the MCE:

Need to reinsert this table from Jesse's document

Name	Colour	Source	Function	Comment
POWER	Green	Connected to power and ground	Power indicator for the TURBOMCE	-
LCA.FAULT	Red	LCA.DONE/ pin	Lit when LCA is not programmed properly	-
RESET	Red	TURBOMCE RESET line	Reset indicator	-
HEARTBT[1]	Green	RMC (PE3) of TURBOMCE	Heartbeat – indicate mode that TURBOMCE is in (BBR, BOOT, MAIN)	Firmware controllable
IDLE	Green	AVEC (PE2) of TURBOMCE	Idle – indicates processor idle time	Firmware controllable
INTR	Yellow	SIZ0 (PE6) of TURBOMCE	Interrupt – turns on when processor is in interrupt	Firmware controllable

[1] Heartbt flashes at 1Hz when main code is loaded and at 2Hz when in boot mode. Heartbt and Idle flash at 1Hz when the MCE is doing a power-on-self-test (POST).

			routine	
SERVC	Red	SIZ1 (PE7) of TURBOMCE	Service – formerly debug LED, General purpose or Service	Firmware controllable

The four firmware controllable LEDs have standardized functions across different boards.

MCE – Engine Control

This section describes the sensors, control and actuators for the mainscan and subscan directions (carriage and drum). This section does not include sensors and actuators other than those used directly with the drum and carriage.

Discrete photo-interruptor Home and Away sensors

Carriage amplifier interface

Drum motor interface

Tach Encoder interface

PLL synthesizer that runs up to 4Mhz

Home and Away Sensors

The new Home and Away sensors replace the Home and Away board that was mounted on the carriage, the opto-interruptors that detected status, and the microswitches that detected over limits. The new sensors are discrete photointerruptors mounted on either end of the carriage track. They are routed to the Xilinx to provide a faster I/O response time than if they went through the SPI bus.

The emitters of the sensors are pulled high using 10K resistors. When the sensor is operating normally, the light from the LED causes the sensor to conduct, pulling the emitter and the imput to the Schmitt inverter to logic low. When the light path is interrupted or the cable is not plugged in, the 10K resistor pulls the input high. (schematic)

The cathodes of the LED's are sensed to determine whether the sensors are connected. When current is flowing and an LED is operating properly, the LED voltage drop of ~1.5V pulls the input high to 3.5V. This method of power detect does not use any additional cables or connectors.

Note that the old Home and Away connector is NOT implemented on the MCE board (i.e. you cannot plug the old home and away board into the MCE).

Carriage Amplifier Interface

- Moves the carriage, slaving to the PLL when plotting.
- Provides +/-5V sin/cos values for carriage amp I and Q phases.
- Passes carriage status to the processor, and provides carriage enable.

The sine and cosine analog outputs are driven by a 12-bit serial DAC. The DAC is the same one used by the Drum Amp spare analog output, except that it is connected to the LCA instead of the SPI bus because it must run much faster (10MHz) than the SPI bus (1MHz). (schematic)

The carriage amplifier interface circuitry has built-in loop back testing capability on the sine and cosine analog signals. The outputs from the op-amps to the carriage amp are looped-back to the on-board A/D converter, so the integrity of part of the carriage amp interface can be verified by firmware.

Power

The following table gives the pinouts of the power connector. This configuration gives the greatest flexibility. If the carriage amp has to be safety isolated, it can generate its own +12V, -12V and +5V supply from +24V.SAFE or +48V.SAFE.

J13 (CA_PWR) MINI-UML 3X3

Pin	Name	Function	Comment
1	+24V.SAFE	Safe +24V	Unused in current carriage amp
2	RTN	Ground return	-
3	+48V.SAFE	Safe +48V	Used to drive carriage
4	RTN	Ground return	-
5	CHASSIS	Shielding	-
6	RTN	Ground return	-
7	-12V	-12V supply from MCE	-
8	+12V	+12V supply from MCE	-
9	+5V	+5V supply from MCE	-

The following table shows the physical layout of the pins in the 3X3 mini-UML connector. The pins are positioned this way to provide safety isolation between the safe and unsafe power supply pins

3 +48V.SAFE	2 RTN	1 +24V.SAFE
6 RTN	5 CHASSIS	4 RTN
9 +5V	8 +12V	7 –12V

.

Carriage Amp Faults

The following table lists the outputs of the FAULT and STATUS[0..1] lines, and the associated fault conditions.

FAULT	STATUS 1	STATUS 0	Fault Condition	Comment
0	X	X	No current fault	Status bits could be latched
1	1	1	No +5V	-
1	1	0	Over-temperature (OT) error	-
1	0	1	Over-current (OC) error	-
1	0	0	Low voltage on the +/-12V, +48V rails (UV+(OT&OC)) or combination or errors.	-

The STATUS[0..1] lines are latched on the carriage amp, but the FAULT line is not. The FAULT line is only active whenever the carriage is in a fault condition. The MCE must read the STATUS[0..1] lines and assert the CLEAR/ line to clear the fault. As a result of the combination logic on the latched status, it is impossible to distinguish between low voltage condition, or a combination of over-temperature and over-voltage error.

The carriage amp also has a reset monitor, which clears the status latches if the 5V supply voltage drops below 4.75V. If the FAULT condition is present but the status lines are both 0, it means that the +5V supply to the amp is low or missing.

Drum Amplifier Interface

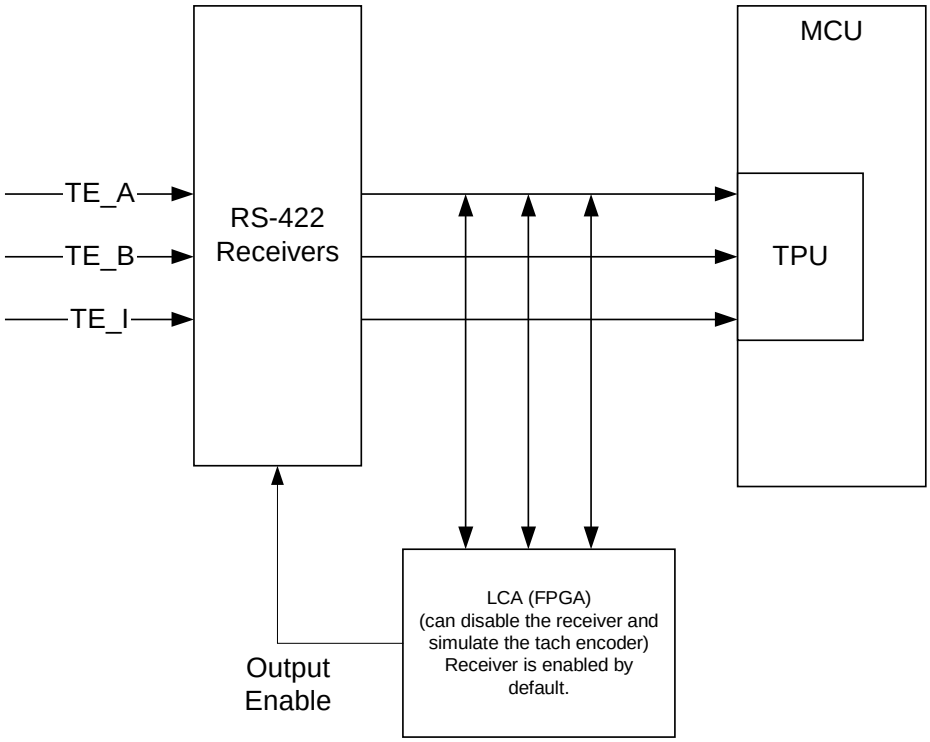
Provides a flexible interface for the current Automotion Drum Amp, and for any future Drum Amp (single ±10V or ±2V analog output; digital input and output channels). The interface has a pulse-width modulated channel, and also an currently unused analog output. Since the interface on the MCE is not insulated, the drum amp must provide reinforced insulation.

The analog output of the Drum Amp can be set to either +/-2V or +/-10V, with 12-bit resolution. Installing J45 produces 10V output, removing J45 produces 2V output. The drum amplifier analog circuitry has built-in loop back testing capability. The output to the drum amp is looped-back to the on-board A/D converter, so the integrity of part of the analog part of the drum amp interface can be verified by firmware.

Tach Encoder

The MCE board supports the Heidenhain encoder as well as the old Creo 9000 line encoder. It interfaces to a 15 pin female mini-DSUB connector on the MCE board (J20). This connector supplies +5V power to the encoder, and receives three RS-422 differential inputs A, B and I (index).

The output of the RS-422 receivers connect to TPU0, TPU1 And TPU2 of the MCU, as well as to three pins of the Xilinx FPGA. The RS-422 receivers can be disabled, allowing the LCA to simulate the Tach encoder and drive the MCU pins directly.



PLL Synthesizer within LCA

Receives TACH pulses from the drum and generates SCLK (pixel line-rate).

MCE – Generic Engine IO

This section describes the sensors and actuators that provide plate handling capabilities as well as the other sensors necessary for system diagnostics. (Must be able to tell whether each and every cable is connected - cable detect, presence detect, or voltage level.)

Analog

- **1 onboard temperature sensor**
- **3 Thermistor temperature inputs**
- **1 700kPa pressure sensor (system pressure)**
- **1 100kPa pressure sensor (drum vacuum)**
- **1 spare 4-20mA analog input (**pressure sensor expansion port)

Digital

- **16 solenoid outputs (24V open-drain, 225 mA, safety-switched)**
- **3 relay outputs (24V open-drain, 225 mA, not safety-switched)**
- **24 generic digital inputs (photo-interrupter/switch/other)**

Analog

Onboard Temperature Sensor

The MCE board measures the ambient (onboard) temperature so that if the board or the enclosure overheats - then what. How does this relate to firmware??

Frame, Lead screw and Carriage Thermistor Inputs

- Three channels for thermistor input on J30.
- Another channel for the lead-screw temperature and cable detect also provided on J36. Reduces cabling complexity for the lead screw temperature thermistor to go through the cable track to the carriage Only one of the channels is used.
- Need to know how firmware handles over or under temperature?

J36 (BS_TEMP) Alternate Temperature Sensor Connector MINIFIT2X2			
Pin	Signal Name	IO Type	Description
1 3	PD.LSTEMP+ PD.LSTEMP-	Input	Presence detect for lead-screw temperature sensor cable to the head
2 4	LSTEMP0+ LSTEMP0-	Analog Input, Diff amp.	Lead-screw temperature (into 2k49)

Pressure Sensors

The MCE board has two pressure sensors and a pressure sensor expansion port:

- 1 700kPa pressure sensor (system pressure)
- 1 100kPa pressure sensor (drum vacuum)
- 1 spare 4-20mA analog input (pressure sensor expansion port)

Each of the pressure sensors has dual port differential input. The following diagram illustrates the ports on the pressure sensors. Take care when connecting the pneumatics system to the pressure sensors - connecting to the wrong port might damage the sensors if the pressure exceeds the maximum rated pressure of the sensor.



Digital

The solenoids and relays are driven with power logic 8-bit shift registers. All of the solenoid drivers, relays and actuators are powered on in a “safe” state. When the MCE resets, the enable pin of the driver is pulled high by a resistor to ensure that all of the outputs are disabled until the registers are properly initialized.

Solenoid Output Connector (J10)

The solenoid connector is designed such that the ribbon cable can plug directly into a manifold. Each “channel” of the manifold plugs into one single or double acting solenoid. To drive the single acting solenoid, the signal from only one of the pins is used and for a double acting solenoid, both pins are used. The MCE can support up to 12 solenoids on a single manifold, four of which can be double acting. One 2x13 solenoid connector.provides a total of 16 bits of safety-rated discrete output.

Since the manifold design does not have any spare pins, cable detect is accomplished by taking the double-acting pins of the first two channels and making them the loopback for cable detect. Simply shorting those two pins on the Manifold end signals the MCE that the manifold is connected. As a result of those two pins being used up, the first two channels of the manifold must be single acting.

Relay Output Connector (J24)

Three spare channels on the MCE board can drive off-board relays such as UDRC or chiller control. They are powered off +24V.I signal so that even if the safety loop is broken, the relays still have power.

Sensors

The MCE has 24 channels of generic digital input (includes the Home and Away sensors already described under Engine Control)

- Away-Side Digital Input Connector (J4): The DSUB 37 pin female connector provides 9 channels of digital sensors, 4 of which are connected via an inverting schmitt trigger to the FPGA for fast response.
- Spare Digital Input Connector (J5): The DSUB 25 pin female connector provides 6 channels of digital sensors that are all connected via an inverting schmitt trigger to the FPGA for fast response.
- Home-Side Digital Input Connector (J6): The DSUB 37 pin male connector provides 9 channels of digital sensors, 4 of which are connected via an inverting schmitt trigger to the FPGA for fast response.

Each sensor has a group of 4 wires – two of which power the LED, and the other two that connect across the photodiode. The MCE is capable of detecting the presence of each opto-interruptor sensor individually by measuring the current across the LED.

All of the presence detect signals and some of the input signals are routed to a shift register and interfaced to the SPI bus of the microprocessor. The rest of the input signals are connected via an inverting Schmitt trigger to the FPGA for faster response time than the SPI bus. For example, in the old CTP, the home and away signals used to be on a circuit board with RS422 type interface. On the MCE board, the home and away sensors are counted as part of the generic digital input signals, and they are routed to the channels that go directly into the FPGA.

MCE – Specific Engine IO

1 Plate Flyoff interface

1 load ramp sensor interface

- **digital input**

1 electronic registration interface

- **4 channels**
- **contact or contactless**

1 UIB connection

- **5 lamps/buzzers**
- **1 button**

Plate Flyoff Interface (J19 and J3 for power)

The sensor interfaces to the Plate FlyOff (PFO) detector, which reports an active-high flyoff if the plate cuts across a sensing beam in front of the drum. The 8-pin sensor is backwards compatible with Trendsetter type PFO sensors.

PFO sensors are either LED or laser based. The laser based PFO is generally used for larger distances (such as VLF) or a more specialized application (Spectrum). The LED based sensor is safe to the naked eye, so opening a panel door is not a hazard. But power to the PFO laser must be removed when the panel is opened. A separate 2-pin connector supplying +24V.SAFE and GND is provided for this purpose.

J3 (PFO_E) MINIFIT1X2

Pin	Signal Name	IO Type	Description
1	+24V.SAFE	Power	Safety switched +24V
2	GND	Power	Ground

This extra connector is in the safety area away from the main PFO connector because of creepage and clearance requirements. To make things simpler, there is no cable detect on this optional connector. The absence of the cable (and laser power) would cause a “flyoff” to be detected anyway.

Load Ramp Sensor Interface (J12)

This connector is backwards compatible with Trendsetter type photo-reflective load ramp sensor. It detects the presence or absence of the plate on the load ramp.

Electronic Registration Interface (J21)

Tie in with firmware?

The Electronics Registration board is connected to the MCE by a 2x7 header. Four channels of digital input is provided to interface with open-collector type output.

The actual electronics registration board is either a contact type (i.e. the plate touching registration pins completes the circuit) or of an opto-inductive type (power transmitted to the drum via an inductor, and the signal returned via LED and photodiode pair).

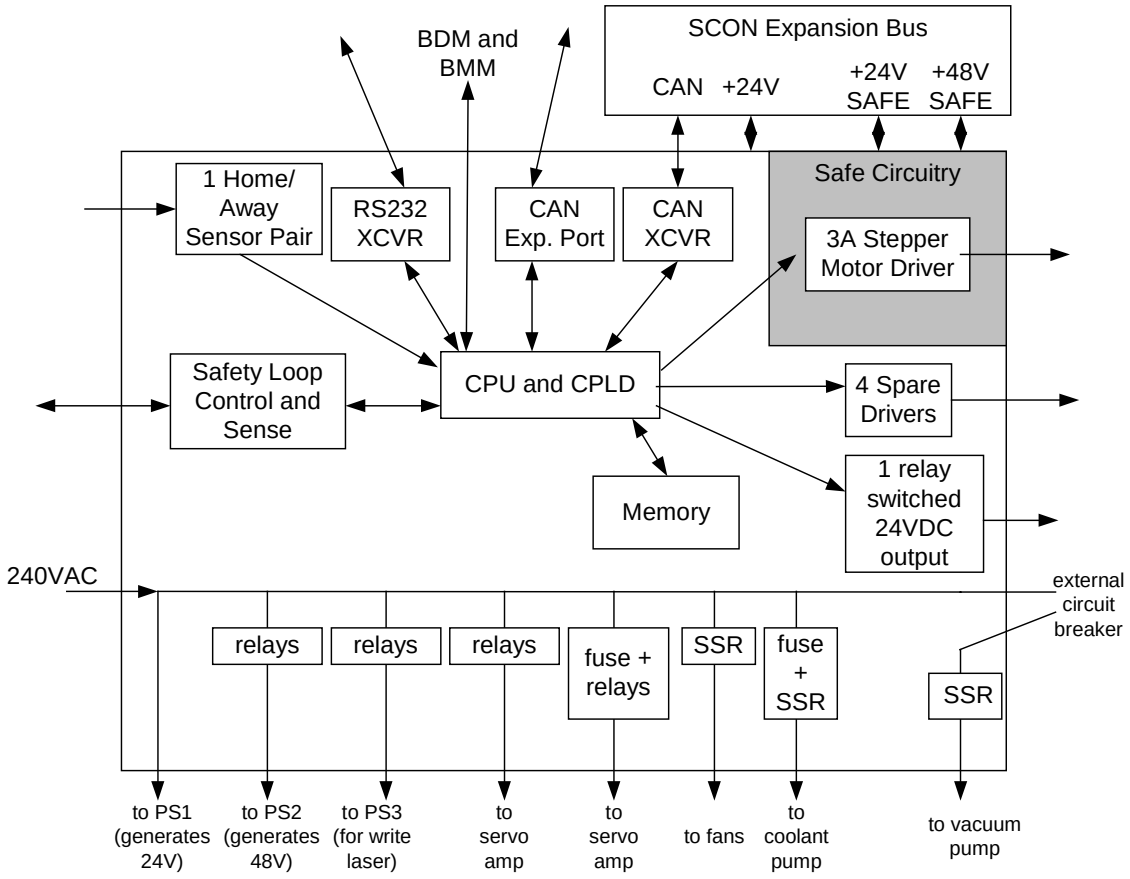
User Interface Board (J16)

The user interface board can have a button, a buzzer, and up to four LEDs. The buzzer and the four LEDs are driven by the same TPIC driver that powers the relay connector.

PDB

Functionality:

- AC distribution
- Safety-loop control
- Head stage control
- High-power DC actuators



PDB – Communications

1 serial port (RS-232)

SCON

1 1MBps CAN communication link

Generates +24V, +24V.SAFE, +48V.SAFE

PDB – Head stage control

3A peak, 48V stepper driver

32 µstep/step micro stepping supported (speed dependant)

Tested, but not currently populated

PDB – Safety Circuit (1/2)

4 separate door loop sensors

2 loops – laser and mechanical

Override (cheater) provided by keyswitch input

Mechanical drum brake support

Solenoid door lock support

- Hardware opening of safety loop on unlock

Class 3 relay system

- Redundant positively guided relays
- Firmware sensed and disabled

24V.SAFE is DC-switched

PDB – DC I/O

4 3A 24V outputs

2 Home-away inputs

PDB – AC IO

All outputs are under firmware control as well as safety loop

All fuses and relay operations are sensed

3 240V Power supply outputs, not fused

- Always on (PS1)
- Mech safe (PS2)
- Write laser safe (PS3)

Mech-loop switched outputs

- Drum amplifier (10A, not fused)
- Safe spare output (6.3A, fused)

Non-safety switched outputs (SSR controlled)

- Vacuum pump (15A, circuit-breaker)
- Fan power (5A, not fused)
- Water pump power (5A, fused)

GENINE

GENINE – Functionality

- Stepper control
- IO

GENINE – Communications

1 serial port (RS-232)

SCON

1 1MBps CAN communication link

Generates +24V, +24V.SAFE, +48V.SAFE

GENINE – Stepper control

Dual stepper motor driver

- 3A stepper controller and driver
- interface for CA stepper driver

GENINE - Digital/analog IO

Digital

- 24 digital inputs (Some on IRB connector)
- 2 2.5A 24V outputs
- 32 Solenoid outputs

Analog

- 1 100kPa pressure sensor
- 1 analog thermistor input (Diff amp)
- 3 4-20mA inputs (Compatible with PSEB/MCE connection)

Architecture - Control

Workstation (Print Console) sends commands to MCE

Other devices semi-intelligent slaves

Architecture - Power 1/2

200 to 240 VAC 50/60Hz

PDB is safety-loop controller

Architecture - Power 2/2

No Transformers Wide input range power supplies and 240V BLDC amp for drum eliminate need

All configurations:

PS1 - 24 V unswitched (255w) 13-5094 LPS255-CEF - stock configured for 24 V, adjustable to 48 V

PS2 - 48 V switched (255w) 13-5094 LPS255-CEF - stock configured for 24 V, [Carl Rueck] adjusted to 48 V

For TH1.7 - Early Production, Trendsetter Base, Autoloader, and Spectrum

PS3 - 48 V switched - TH WL (400w) 13-4832 MP4

PS4 - 48 V unswitched - TH logic (400w) 13-4832 MP4

For TH2.0 (Single head) - Trendsetter NEWS, Base, Autoloader

PS3 - 48 V switched - TH WL (400w) 13-4832 MP4

PS4 - 48 V unswitched - TH logic (600w) 13-4791 MP6

For TH2.0 - HYDRA

PS3 - 48 V switched - TH WL (600w) 13-4791 MP6

PS4 - 48 V unswitched - TH logic(1000w) 13-5165 MP1

-

Architecture - Safety

Brake added to drum motor

Dual-redundant force-guided relays

Meet reinforced creepage/clearance for European safety requirements

Service override for mechanical hazards, no override for write laser

SCON distributes:

- +24V
- +24V.SAFE
- +48V.SAFE

Nomenclatures

ALE	Autoloader Electronics (board)
BBR	Boot Block Recovery code
BMM	Bootstrap Memory Module (board)
CAN	Controller Area Network (network specification)
CPLD	Complex Programmable Logic Device (Xilinx CPLD)
CTM	Configurable Timer Module
CTP	Computer to Plate
DNE	Data Node Electronics (board)
DOP	Digital Offset Press
FDPE	Fast Data Path Electronics (board)
FPGA	Field Programmable Gate Array
GENINE	GENeric Input/Output Node Electronics (board)
ICE	Imaging Control Electronics (board)
ICT	In Circuit Testing
LCA	The Xilinx Virtex FPGA
LUE	Load Unload Electronics (board)
MCE	Master Control Electronics (board)
MCU	Microcontroller Unit
MPE	Master Processor Electronics (board)
PCU	Programmable Control Unit (the Xilinx FPGA, same as LCA)
PDB	Power Distribution Board
PLL	Phase-Lock Loop
PS2	PlateSetter II
QSM	Queued Serial Module (on MCU)
QSPI	Queued Serial Peripheral Interface (on MCU)
RIP	Raster Image Processor
SCON	Satellite Control (specifications)
SPI	Serial Peripheral Interface
TEE	Trendsetter Engine Electronics (board)
TPG	Test Pattern Generator (RAM)
TPU	Timer Processor Unit (on MCU)
UART	Universal Asynchronous Receiver Transmitter