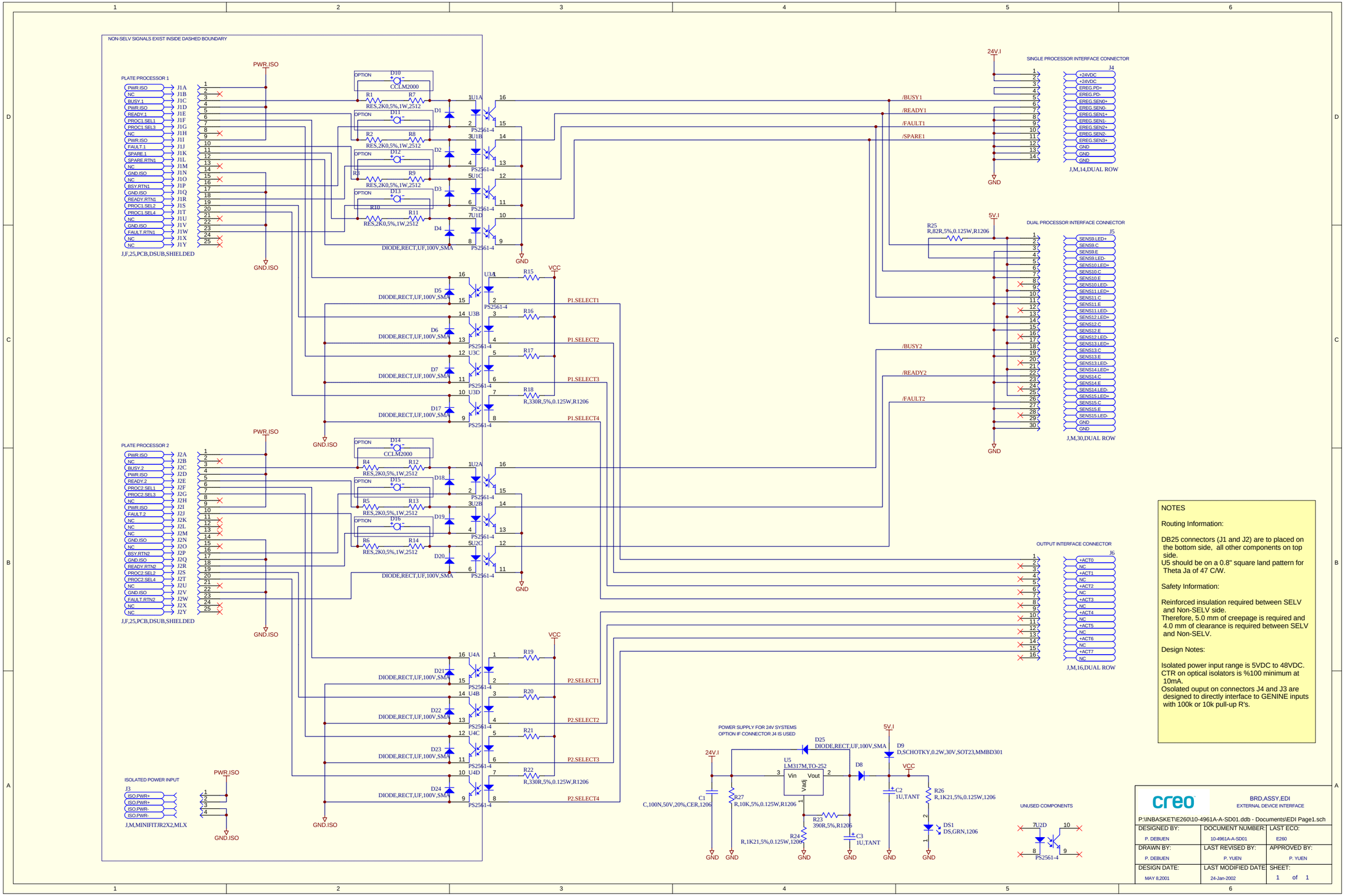

NON-SELV SIGNALS EXIST INSIDE DASHED BOUNDARY
PLATE PROCESSOR 1
PWR.ISO
NC
BUSY.1
PWR.ISO
READY.1
PROC1.SEL1
PROC1.SEL3
NC
PWR.ISO
FAULT.1
SPARE.1
SPARE.RTN1
NC
GND.ISO
NC
BSY.RTN1
GND.ISO
READY.RTN1
PROC1.SEL2
PROC1.SEL4
NC
GND.ISO
FAULT.RTN1
NC
NC
J1A J1B J1C J1D J1E J1F J1G J1H J1I J1J J1K J1L J1M J1N J1O J1P J1Q J1R J1S J1T J1U J1V J1W J1X J1Y
J,F,25,PCB,DSUB,SHIELDED
PWR.ISO
GND.ISO
OPTION
D10
CCLM2000
R1
R7
RES,2K0,5%,1W,2512
D1
1U1A
PS2561-4
D11
R2
R8
D2
3U1B
D12
R3
R9
D3
5U1C
D13
R10
R11
D4
7U1D
DIODE,RECT,UF,100V,SMA
GND
VCC
D5
U3A
R15
P1.SELECT1
D6
U3B
R16
P1.SELECT2
D7
U3C
R17
P1.SELECT3
D17
U3D
R18
R,330R,5%,0.125W,R1206
P1.SELECT4
PLATE PROCESSOR 2
PWR.ISO
NC
BUSY.2
PWR.ISO
READY.2
PROC2.SEL1
PROC2.SEL3
NC
PWR.ISO
FAULT.2
NC
NC
GND.ISO
NC
BSY.RTN2
GND.ISO
READY.RTN2
PROC2.SEL2
PROC2.SEL4
NC
GND.ISO
FAULT.RTN2
NC
NC
J2A J2B J2C J2D J2E J2F J2G J2H J2I J2J J2K J2L J2M J2N J2O J2P J2Q J2R J2S J2T J2U J2V J2W J2X J2Y
J,F,25,PCB,DSUB,SHIELDED
D14
CCLM2000
R4
R12
D18
U2A
R5
R13
D19
U2B
R6
R14
D20
U2C
D21
U4A
R19
P2.SELECT1
D22
U4B
R20
P2.SELECT2
D23
U4C
R21
P2.SELECT3
D24
U4D
R22
R,330R,5%,0.125W,R1206
P2.SELECT4
ISOLATED POWER INPUT
J3
ISO.PWR+
ISO.PWR+
ISO.PWR-
ISO.PWR-
J,M,MINIFITJR2X2,MLX
SINGLE PROCESSOR INTERFACE CONNECTOR
24V.I
J4
+24VDC
+24VDC
EREG.PD+
EREG.PD-
EREG.SEN0+
EREG.SEN0-
EREG.SEN1+
EREG.SEN1-
EREG.SEN2+
EREG.SEN2-
EREG.SEN3+
GND
GND
GND
J,M,14,DUAL ROW
/BUSY1
/READY1
/FAULT1
/SPARE1
DUAL PROCESSOR INTERFACE CONNECTOR
5V.I
R25
R,82R,5%,0.125W,R1206
J5
SENS9.LED+
SENS9.C
SENS9.E
SENS9.LED-
SENS10.LED+
SENS10.C
SENS10.E
SENS10.LED-
SENS11.LED+
SENS11.C
SENS11.E
SENS11.LED-
SENS12.LED+
SENS12.C
SENS12.E
SENS12.LED-
SENS13.LED+
SENS13.C
SENS13.E
SENS13.LED-
SENS14.LED+
SENS14.C
SENS14.E
SENS14.LED-
SENS15.LED+
SENS15.C
SENS15.E
SENS15.LED-
GND
GND
J,M,30,DUAL ROW
/BUSY2
/READY2
/FAULT2
OUTPUT INTERFACE CONNECTOR
J6
+ACT0
NC
+ACT1
NC
+ACT2
NC
+ACT3
NC
+ACT4
NC
+ACT5
NC
+ACT6
NC
+ACT7
NC
J,M,16,DUAL ROW
POWER SUPPLY FOR 24V SYSTEMS
OPTION IF CONNECTOR J4 IS USED
24V.I
D25
DIODE,RECT,UF,100V,SMA
U5
LM317M,TO-252
Vin
Vout
Vadj
D8
5V.I
D9
D,SCHOTKY,0.2W,30V,SOT23,MMBD301
VCC
C1
C,100N,50V,20%,CER,1206
R27
R,10K,5%,0.125W,R1206
R23
390R,5%,R1206
R24
R,1K21,5%,0.125W,1206
C3
1U,TANT
C2
1U,TANT
R26
R,1K21,5%,0.125W,1206
DS1
DS,GRN,1206
GND
UNUSED COMPONENTS
7U2D
PS2561-4
NOTES
Routing Information:
DB25 connectors (J1 and J2) are to placed on the bottom side, all other components on top side.
U5 should be on a 0.8" square land pattern for Theta Ja of 47 C/W.
Safety Information:
Reinforced insulation required between SELV and Non-SELV side.
Therefore, 5.0 mm of creepage is required and 4.0 mm of clearance is required between SELV and Non-SELV.
Design Notes:
Isolated power input range is 5VDC to 48VDC.
CTR on optical isolators is %100 minimum at 10mA.
Osolated ouput on connectors J4 and J3 are designed to directly interface to GENINE inputs with 100k or 10k pull-up R's.
creo
BRD,ASSY,EDI
EXTERNAL DEVICE INTERFACE
P:\INBASKET\E260\10-4961A-A-SD01.ddb - Documents\EDI Page1.sch
DESIGNED BY: P. DEBUEN
DOCUMENT NUMBER: 10-4961A-A-SD01
LAST ECO: E260
DRAWN BY: P. DEBUEN
LAST REVISED BY: P. YUEN
APPROVED BY: P. YUEN
DESIGN DATE: MAY 8,2001
LAST MODIFIED DATE: 24-Jan-2002
SHEET: 1 of 1