LIONEL (Little Input Output Node ELectronics) 10-4801B

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Notes:

Traces with special current requirements are noted in red. Modify trace thickness for external/internal layers and copper thickness.
Traces should be capable of withstanding twice the rated current for 1 minute.
Unless otherwise noted, assume traces will carry 100mA continuous current maximum (200mA for 1 minute).
Trace thickness should be 8mils minimum (2oz copper).

Do not split ground plane.

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LIONEL Schematic
Top Sheet
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DESIGNED BY:	DOCUMENT NUMBER:	
J. Malm	713-04801B-E	
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
J. Malm	Dean Lowe	Dean Lowe
DESIGN DATE:	LAST MODIFIED DATE	SHEET:
July 8, 2000	October 31,2003	1 of 7

Analog Circuitry

MODA and MODB must be low during reset for proper operation.

Ports G and H configured for pulldown.

Place series termination resistors as close to the microcontroller as possible.

When reset is pushed, all LEDS will turn on due to pullups on the NOT gate inputs.

BDM (Background Debug Module) Connector. Label on board BDM

BOOT Jumper Label on board BOOT

Second CAN controller (CAN1) is only for DG128 and if D60 is installed, pins 102 (CAN1.TXD) and 103 (CAN1.RXD) will be used as General Purpose I/O.

LIONEL Schematic Microcontroller CREO Confidential		
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DESIGNED BY: J. Malm	DOCUMENT NUMBER: 713-04801B-E	LAST ECO:
DRAWN BY: J. Malm	LAST REVISED BY: Dean Lowe	APPROVED BY: Dean Lowe
DESIGN DATE: July 10, 2000	LAST MODIFIED DATE: October 31.2003	SHEET: 2 of 7

16 Digital Inputs, Assembly/Version Registers

Digital Input Connector #1
Plate Registration
Label on board DIG_IN1

J11
+24V
+24V
EREG.PD+
EREG.PD-
EREG.SEN-
EREG.SEN
EREG.SEN+
EREG.SEN-
EREG.SEN+
EREG.SEN-
NC
NC
J,M,14,DUAL ROW

+24V.FUSED
VCC.FUSED
VCC
C79 C,10N
C78 C,10N
CHASSIS
C83 C,10N
C62 C,10N
CHASSIS
GND
RN12D RN,100K
RN12C RN,100K
RN12B RN,100K
RN12A RN,100K
RN14B RN,10K
RN10A RN,10K
RN10B RN,10K
RN10C RN,10K
RN10D RN,10K
PD.PLATEREG
PLATEREG0
PLATEREG1
PLATEREG2
PLATEREG3
D49 OMIT C,10N
GND CHASSIS
RN14A RN,10K
GND
D48 OMIT C,10N
GND CHASSIS
D40 OMIT C,10N
GND CHASSIS
D47 OMIT C,10N
GND CHASSIS
D42 OMIT C,10N
GND CHASSIS

Pin 14 is Removed on this connector for Keying

Digital Input Connector #2
Label on board DIG_IN2

J7
SENS4.LED+
SENS4.C
SENS4.E
SENS4.LED-
SENS5.LED+
SENS5.C
SENS5.E
SENS5.LED-
SENS6.LED+
SENS6.C
SENS6.E
SENS6.LED-
SENS7.LED+
SENS7.C
SENS7.E
SENS7.LED-
SENS8.LED+
SENS8.C
SENS8.E
SENS8.LED-
J,M,20,DUAL ROW SAMTEC

GND CHASSIS
D35 OMIT C,10N
C59 C,10N
D27 OMIT C48 C,10N
C,10N C27
VCC.FUSED
C52 C,10N
CHASSIS
D31 OMIT C55 C,10N
D29 OMIT C50 C,10N
D25 OMIT C44 C,10N
VCC
RN6D RN,100K
RN6C RN,100K
RN6B RN,100K
RN6A RN,100K
RN7A RN,100K
RN4A RN,10K
RN3A RN,10K
RN4B RN,10K
RN3B RN,10K
RN4C RN,10K
RN3C RN,10K
RN4D RN,10K
RN3D RN,10K
RN5D RN,10K
RN2A RN,10K
SENS4
SENS5
SENS6
SENS7
SENS8
U4A IC,74HCT14
U4F IC,74HCT14
U4B IC,74HCT14
U4E IC,74HCT14
U4C IC,74HCT14
SCD4
SCD5
SCD6
SCD7
SCD8
C54 C,10N
C23 C,10N
CHASSIS
D16 OMIT C22 C,10N
GND CHASSIS
D20 OMIT C29 C,10N
GND CHASSIS
D22 OMIT C40 C,10N
GND CHASSIS
D17 OMIT C24 C,10N
GND CHASSIS
D21 OMIT C32 C,10N
GND CHASSIS
R47 R,221R
R37 R,221R
R2 R,221R
R1 R,221R
R30 R,221R
GND

PD.PLATEREG [2]
PLATEREG[0..3] [2]
SCD[4..15] [2,6]
SENS[4..15] [2]

Digital Input Connector #3
Label on board DIG_IN3

J8
SENS9.LED+
SENS9.C
SENS9.E
SENS9.LED-
SENS10.LED+
SENS10.C
SENS10.E
SENS10.LED-
SENS11.LED+
SENS11.C
SENS11.E
SENS11.LED-
SENS12.LED+
SENS12.C
SENS12.E
SENS12.LED-
SENS13.LED+
SENS13.C
SENS13.E
SENS13.LED-
SENS14.LED+
SENS14.C
SENS14.E
SENS14.LED-
SENS15.LED+
SENS15.C
SENS15.E
SENS15.LED-
GND
GND
J,M,30,DUAL ROW

VCC.FUSED
C65 C,10N
C39 C,10N
CHASSIS
C64 C,10N
C35 C,10N
CHASSIS
GND
GND CHASSIS
D45 OMIT C70 C,10N
D43 OMIT C71 C,10N
D15 OMIT C60 C,10N
D33 OMIT C56 C,10N
D38 OMIT C63 C,10N
D24 OMIT C57 C,10N
D39 OMIT C53 C,10N
VCC
RN9D RN,100K
RN9C RN,100K
RN9B RN,100K
RN9A RN,100K
RN7D RN,100K
RN7C RN,100K
RN7B RN,100K
RN8A RN,10K
RN2B RN,10K
RN8B RN,10K
RN2C RN,10K
RN8C RN,10K
RN2D RN,10K
RN8D RN,10K
RN1A RN,10K
RN5A RN,10K
RN1B RN,10K
RN5B RN,10K
RN1C RN,10K
RN5C RN,10K
RN1D RN,10K
SENS9
SENS10
SENS11
SENS12
SENS13
SENS14
SENS15
U4D IC,74HCT14
U2F IC,74HCT14
U2A IC,74HCT14
U2E IC,74HCT14
U2B IC,74HCT14
U2C IC,74HCT14
U2D IC,74HCT14
SCD9
SCD10
SCD11
SCD12
SCD13
SCD14
SCD15
D23 OMIT C28 C,10N
D28 OMIT C42 C,10N
D32 OMIT C47 C,10N
D36 OMIT C51 C,10N
D26 OMIT C36 C,10N
D30 OMIT C41 C,10N
D34 OMIT C49 C,10N
R34 R,221R
R27 R,221R
R25 R,221R
R23 R,221R
R26 R,221R
R24 R,221R
R22 R,221R
GND

Analog Circuitry

Version Register

+5V_A
Resistor "3"
Resistor "2"
Resistor "1"
Resistor "0"
R16 OMIT
R15 OMIT
R14 OMIT
R13 OR JUMPER
VREG3
VREG2
VREG1
VREG0
VREG[0..3] [2]
RN21D RN,10K
RN21C RN,10K
RN21A RN,10K
RN21B RN,10K
GND

Version register located in analog section.

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LIONEL Schematic
Digital Inputs, Version Register
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DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
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J. Malm	Dean Lowe	Dean Lowe
DESIGN DATE:	LAST MODIFIED DATE	SHEET:
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Analog Circuitry

Note:
Do not split GND plane. The OPTOREFL inputs are single-ended and ground loops will form if the GND plane is split.

Off-board Temperature (Analog) Sense

Temperature Sensor Input Port (thermistor) Label on Board TEMP

J21 +5VDC, GND, TEMP+, TEMP-, PD.TEMP+, PD.TEMP- — J,M,6,PCB,MINI-MATE-N-LOCK

VCC.FUSED — C137 C,10N — CHASSIS

GND CHASSIS — D59 OMIT — C119 C,10N

+5V.A — R78 R,2K49 — R77 R,100K,1% — U14A IC,LT1013DID

C132 C,10N — R76 R,100K,1% — GND

R83 R,100K,1% — R86 R,2K49 — GND

R82 R,100K,1% — C131 C,10N

RN26A RN,10K — C100 CP,22U,20V — GND — TEMP.EXT — TEMP.EXT [2]

CHASSIS — C134 C,10N — GND — D56 OMIT — C106 C,10N — GND CHASSIS

D55 OMIT — C122 C,10N — GND CHASSIS

RN27B RN,10K — RN27A RN,10K — GND — PD.TEMP — PD.TEMP [2]

This amplifier is a 1st order LPF:
TEMP.EXT(s) = (TEMP+ - TEMP-)*(1/(1+100K*10n*s))
= (TEMP+ - TEMP-)*(1/(1+1e-3*s))

For the connectors below, jumper Pins 3 and 5 for Cable Detect; Pin 6 to remain unused.

4-20mA (0-5V) Analog Inputs

Analog Input Port 1 (4-20mA or 0-5V) Label on Board AN_1

J17 — J,M,6,SINGLE ROW,LOCKING

C135 C,10N — +24V.FUSED — CHASSIS — CHASSIS — C105 C,10N — GND

VCC.FUSED

GND CHASSIS — D44 OMIT — C136 C,10N

GND CHASSIS — D37 OMIT — C130 C,10N

GND CHASSIS — D46 OMIT — C120 C,10N

RN26B RN,10K — R85 R,221R — C45 CP,22U,20V — GND

+5V.A — GND — D11 D,DUAL,BAT54 — OPTOREFL0

RN27D RN,10K — RN27C RN,10K — GND

+5V.A — GND — D6 D,DUAL,BAT54 — OPTOPD0

OPTOREFL[0..2] — OPTOREFL[0..2] [2]

OPTOPD[0..2] — OPTOPD[0..2] [2]

Analog Input Port 2 (4-20mA or 0-5V) Label on Board AN_2

J16 — J,M,6,SINGLE ROW,LOCKING

C111 C,10N — +24V.FUSED — CHASSIS — CHASSIS — C128 C,10N — GND

VCC.FUSED

RN26C RN,10K — R81 R,221R — C73 CP,22U,20V — GND

+5V.A — GND — D10 D,DUAL,BAT54 — OPTOREFL1

RN24B RN,10K — RN24A RN,10K — GND

+5V.A — GND — D8 D,DUAL,BAT54 — OPTOPD1

Analog Input Port 3 (4-20mA or 0-5V) Label on Board AN_3

J14 — J,M,6,SINGLE ROW,LOCKING

C85 C,10N — +24V.FUSED — CHASSIS — CHASSIS — C97 C,10N — GND

VCC.FUSED

RN26D RN,10K — R74 R,221R — C98 CP,22U,20V — GND

+5V.A — GND — D9 D,DUAL,BAT54 — OPTOREFL2

RN24D RN,10K — RN24C RN,10K — GND

+5V.A — GND — D7 D,DUAL,BAT54 — OPTOPD2

D19 OMIT — C104 C,10N — GND CHASSIS

D52 OMIT — C133 C,10N — GND CHASSIS

D41 OMIT — C88 C,10N — GND CHASSIS

+48V.SAFE — R53 R,20K — 48VRES0 — R52 R,20K — R84 R,3K3 — C114 C,100N — GND

RN25A RN,10K — +5V.A — GND — D14 D,DUAL,BAT54 — 48VSAFE.DET — 48VSAFE.DET [2]

+48VSAFE.DET = 0.076 X (+48V.SAFE)
= 3.66V @ 48V.

+24V.SAFE — R65 R,20K — 24VRES0 — R58 R,20K — R80 R,7K68 — C113 C,100N — GND

RN25B RN,10K — +5V.A — GND — D13 D,DUAL,BAT54 — 24VSAFE.DET — 24VSAFE.DET [2]

+24VSAFE.DET = 0.161 X (+24V.SAFE)
= 3.87V @24V.

+24V — R70 R,20K — R71 R,20K — R79 R,7K68 — C112 C,100N — GND

RN25C RN,10K — +5V.A — GND — D12 D,DUAL,BAT54 — 24V.DET — 24V.DET [2]

+24V.DET = 0.161 X (+24V)
= 3.87V @24V.

VCC — R68 R,10K0 — RN25D RN,10K — C102 C,100N — GND — VCC.DET — VCC.DET [2]

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LIONEL Schematic
Analog Inputs
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DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
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DRAWN BY:	LAST REVISED BY:	APPROVED BY:
J. Malm	Jesse Malm	Jesse Malm
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
July 8, 2000	November 23, 2001	4 of 7

All circuitry within this dashed line requires 2.4mm creepage and clearance (0.5mm inner layer) to all other circuitry on the same layer.

Digital Outputs (open-drain)

[7] MFDSAFE.VCC

MFDSAFE.24V
C18 C,10N CHASSIS
C11 C,10N CHASSIS

2A Current
F2 +24V OMIT
F1 +24V.SAFE F,POLYSWITCH,0.90A

Install F1 OR F2 (not both)

[2] SPI.CS/[0..3] → SPI.CS/[0..3]
SPI.CS/0 R8 R,470R,1206 MFDRES0 R3 R,470R,1206 MFDSAFE.CS/0
[2] SPI.SCK1 R10 R,470R,1206 MFDRES1 R5 R,470R,1206 MFDSAFE.SCK1
[2] SPI.MOSI R35 R,470R,1206 MFDRES2 R28 R,470R,1206 MFDSAFE.MOSI

U1A
9 G (ENABLE)
12 RCK
8 SRCLR
13 SRCK
3 SER IN
DRAIN0 4
DRAIN1 5
DRAIN2 6
DRAIN3 7
DRAIN4 14
DRAIN5 15
DRAIN6 16
DRAIN7 17
SER OUT 18
IC,TPIC6595

MFDSAFE.G/ R20 R,10K0 GND

CHASSIS CHASSIS CHASSIS CHASSIS
C10 C,10N
C12 C,10N
C13 C,10N
C14 C,10N

C19 C,10N
C17 C,10N
C16 C,10N
C15 C,10N
CHASSIS CHASSIS CHASSIS CHASSIS

0.25A Current MFDSAFE.ACT0 → J2 1
0.25A Current MFDSAFE.ACT1 → 3
0.25A Current MFDSAFE.ACT2 → 5
0.25A Current MFDSAFE.ACT3 → 7
0.25A Current MFDSAFE.ACT4 → 9
0.25A Current MFDSAFE.ACT5 → 11
0.25A Current MFDSAFE.ACT6 → 13
0.25A Current MFDSAFE.ACT7 → 15

J,M,16,DUAL ROW SAMTEC

ACT0- 2 +24V
ACT1- 4 +24V
ACT2- 6 +24V
ACT3- 8 +24V
ACT4- 10 +24V
ACT5- 12 +24V
ACT6- 14 +24V
ACT7- 16 +24V

Solenoid Driver Output Port (open-drain)
Label on Board SOL_DRV1

R4 R,10K,1206 MFDRES3 R9 R,10K,1206
R31 R,10K,1206 MFDRES4 R48 +24V R,10K,1206

VCC D3 D,DUAL,BAT54 GND
PD.MFD1 → PD.MFD1 [2]
RN17A RN,10K GND

All circuitry within this dashed line requires 2.4mm creepage and clearance (0.5mm inner layer) to all other circuitry on the same layer.

PWM Outputs (open-drain)

[2] PWMOUT[0..5] → PWMOUT[0..5]
PWMOUT0 R51 R,470R,1206 PWMRES0 R43 R,470R,1206 PWMSAFE.PWM0
PWMOUT1 R49 R,470R,1206 PWMRES1 R42 R,470R,1206 PWMSAFE.PWM1
PWMOUT2 R44 R,470R,1206 PWMRES2 R41 R,470R,1206 PWMSAFE.PWM2
PWMOUT3 R40 R,470R,1206 PWMRES3 R39 R,470R,1206 PWMSAFE.PWM3
PWMOUT4 R87 R,470R,1206 PWMRES4 R88 R,470R,1206 PWMSAFE.PWM4
PWMOUT5 R50 R,470R,1206 PWMRES5 R32 R,470R,1206 PWMSAFE.PWM5

U3
IC,TPIC2601
G1 G2 G3 G4 G5 G6
DRAIN1 DRAIN2 DRAIN3 DRAIN3 DRAIN4 DRAIN5 DRAIN6
GND TAB I6 GND

CHASSIS CHASSIS
C26 C,10N
C31 C,10N

C4 C,10N
C7 C,10N
CHASSIS CHASSIS

C20 C,10N
C21 C,10N
CHASSIS CHASSIS

C5 C,10N CHASSIS
C6 C,10N
C8 C,10N CHASSIS

2.5A Current PWMSAFE.24V1
F6 +24V F,POLYSWITCH,2.50A
F4 +24V.SAFE OMIT
F5 +24V F,POLYSWITCH,2.50A
F3 +24V.SAFE OMIT

Install F5 and F4, OR F6 and F3. Bend 90 degrees to avoid interference with connectors.

C30 C,10N CHASSIS

1A Current PWMSAFE.PWMD0
1A Current PWMSAFE.PWMD1
1A Current PWMSAFE.PWMD2
1A Current PWMSAFE.PWMD3
1A Current PWMSAFE.PWMD4
1A Current PWMSAFE.PWMD5

1 +24V J5A J,M,MINIFITJR2X3
4 PWM0- J5D J,M,MINIFITJR2X3
2 +24V J5B J,M,MINIFITJR2X3
5 PWM1- J5E J,M,MINIFITJR2X3
3 PD.PWM0+ J5C J,M,MINIFITJR2X3
6 PD.PWM- J5F J,M,MINIFITJR2X3

PWM Output Port 1 (open-drain, 1A per channel) Label on Board PWM_OUT1

1 +24V J1A J,M,MINIFITJR2X4
5 PWM2- J1E J,M,MINIFITJR2X4
2 +24V J1B J,M,MINIFITJR2X4
6 PWM3- J1F J,M,MINIFITJR2X4
3 PWM4- J1C J,M,MINIFITJR2X4
7 PWM5- J1G J,M,MINIFITJR2X4
4 PD.PWM1+ J1D J,M,MINIFITJR2X4
8 PD.PWM1- J1H J,M,MINIFITJR2X4

PWM Output Port 2 (open-drain, 1A per channel) Label on Board PWM_OUT2

CHASSIS C37 C,10N
CHASSIS C38 C,10N

PWMSAFE.PD1+ R36 R,10K,1206 PWMRES6 R46 +24V R,10K,1206
PWMSAFE.PD1- R7 R,10K,1206 PWMRES7 R12 R,10K,1206
PWMSAFE.PD2+ R33 R,10K,1206 PWMRES8 R45 +24V R,10K,1206
PWMSAFE.PD2- R6 R,10K,1206 PWMRES9 R11 R,10K,1206

VCC D5 D,DUAL,BAT54 GND
PD.PWM_OUT1 → PD.PWM_OUT1 [2]
RN17C RN,10K GND

Bend 90 degrees to avoid interference with connectors.

VCC D4 D,DUAL,BAT54 GND
PD.PWM_OUT2 → PD.PWM_OUT2 [2]
RN17B RN,10K GND

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LIONEL Schematic
Digital/PWM Outputs

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DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
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J. Malm	Jesse Malm	Jesse Malm
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
July 8, 2000	February 21, 2001	5 of 7

Expansion Bus Connector #1
Label on board: SCON1

J13A
SAT_+48SAFE
SAT_+48RTN
SAT_+24SAFE
SAT_+24SRTN
SAT_+24RTN
SAT_+24V
CHASSIS
J,M,MINIFITJR2X8

9A Current
R72 R,1M00
C96 C,100N CHASSIS
GND

+48V.SAFE
+24V.SAFE
+24V
C74 C,10N,100V
C95 C,10N
C67 C,10N
CHASSIS
D2 D,MBRS360
D18 D,MBRS360
D50 D,MBRS360
GND

Expansion Bus Connector #2
Label on board: SCON2

J9A
SAT_+48SAFE
SAT_+48RTN
SAT_+24SAFE
SAT_+24SRTN
SAT_+24RTN
SAT_+24V
CHASSIS
J,M,MINIFITJR2X5

R55 R,1M00
C61 C,100N

J13B
TERM_DET
J,M,MINIFITJR2X8
TERM_DET
J9B
J,M,MINIFITJR2X5

J13D
CAN_H
CAN_L
J,M,MINIFITJR2X8
CAN0_H
CAN0_L
J9C
J,M,MINIFITJR2X5

J13C
BRD_LOC+
BRD_LOC+
BRD_LOC0-
BRD_LOC1-
BRD_LOC2-
BRD_LOC3-
J,M,MINIFITJR2X8
R73 R,1K5
VCC

CAN TRANSCEIVER 0
SCON COMMUNICATIONS

RN22A RN,10K BD0
RN22B RN,10K BD1
RN22C RN,10K BD2
RN22D RN,10K BD3
RN23A RN,100K
RN23B RN,100K
RN23C RN,100K
RN23D RN,100K
GND

U8A
TXD RXD CANH CANL RS VREF
IC,PCA82C250
CAN0.TXD
CAN0.RXD
[2] CAN0.RXD
BD[3..0] [2]

D53 C118 OMIT C,10N
D57 C129 OMIT C,10N
D51 C99 OMIT C,10N
D54 C110 OMIT C,10N
D58 C127 OMIT C,10N
GND CHASSIS

BD[3..0]

DAUGHTER BOARD CONNECTOR #2
J10
+5V
+5V
CAN.TXD
CAN.RXD
GND
GND
TXD_2
RXD_2
RESET/
SPI.CS/1
SPI.CS/2
SPI.CS/3
SPI.SCK2
SPI.SS
SPI.MOSI
SPI.MISO
J,M,16,DUAL ROW HDR

Note daughter board is an extension of the base board and does not provide decoupling or input protection.

[2] CAN0.TXD
[2] CAN1.TXD
CAN1.TXD
CAN1.RXD
GND
TXD_2
RXD_2

[2,7] RESET/
[2] SPI.CS/[0..3]
[2] SPI.SCK2
[2] SPI.SS
[2] SPI.MOSI
SPI.CS/[0..3]
RESET/
SPI.CS/1
SPI.CS/2
SPI.CS/3
SPI.SCK2
SPI.SS
SPI.MOSI

CAN1.RXD
SPI.MISO
CAN1.RXD [2]
SPI.MISO [2]

RN15D RN,10K
RN15B RN,10K
GND GND

DAUGHTER BOARD CONNECTOR #3

[2,5] PWMOUT[0..3]
PWMOUT[0..3]

[2] 1WIRE.TX

DAUGHTER BOARD CONNECTOR #1
+24V.SAFE
J6 OMIT

J12
+5V
+5V
DFAST0
DFAST1
DFAST2
DFAST3
GND
GND
XIRQ/
IRQ/
PWMOUT0
PWMOUT1
PWMOUT2
PWMOUT3
DAUT.DET0
DAUT.DET1
DAUT.DET2
DAUT.DET3
+24V
+24V
+24V.FUSED
J,M,20,DUAL ROW,HDR

SENS nets are effectively pulled high by a 120K resistor from this point when their digital_in connections are left unconnected.

SENS4
SENS5
SENS6
SENS7
SENS12
SENS13
SENS[4..15] [2,3]
DAUT.DET0
DAUT.DET1
DAUT.DET2
DAUT.DET3
DAUT.DET[0..3] [2]
RN13A RN,10K
RN13B RN,10K
RN13C RN,10K
RN13D RN,10K
GND

[2] UART0.TXD
[2] UART1.TXD
UART0.TXD
UART1.TXD

RS232 Serial Port (RS232 PORT)
Label on Board RS232 PORT

J20A
TXD
RTS
DTR
DCD
RI
J,DB9F,RS232
1WIRE_MOD1
1WIRE_MOD2
C139 C,33P
CHASSIS

J20B
RXD
CTS
DSR
GND
CASE
CASE
J,DB9F,RS232
C138 C,33P
GND
CHASSIS

U12A
C1+ C1- C2+ C2-
V+ V-
T1IN T2IN R1IN R2IN
T1OUT T2OUT R1OUT R2OUT
IC,MAX232EE,SO16
CP,1U0,16V C116
CP,1U0,16V C108
1WIRE_MOD
C117 CP,1U0,16V
C109 CP,1U0,16V
GND
TXD_2
RXD_2

J18 OMIT
J19 OMIT
1WIRE_MOD

To use the 1_WIRE mode, individually jumper both J18 and J19

5k pullup required for 1wire bus
D1 D,DUAL,BAT54
VCC
R19 R,4K99
R21 R,10K0
1WIRE
R18 R,10K0
1WIRE.TX
Q1 Q,3904,SOT23
GND

Dallas 1Wire Port
Label on board 1_WIRE
J3
1_WIRE
GND
J,M,MINIFIT,1X2

1WIRE.RX
1WIRE.RX [2]

UART0.RXD
UART1.RXD
UART0.RXD [2]
UART1.RXD [2]

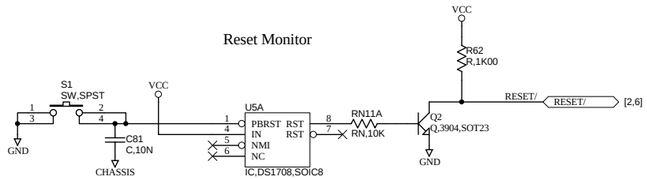
creo

LIONEL Schematic
SCON, Daughter Board, RS232
CREO Confidential
G:\Electrical\HW\Lionel\10-4801B-E\Eng\713-04801B-C-SD01.ddb - Documents\Page 06 Exp_Bus.sch

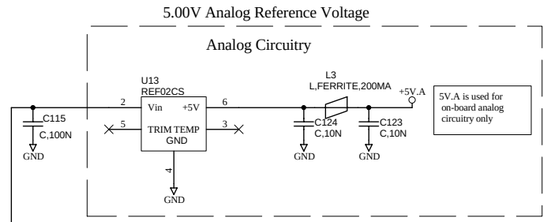
DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
J. Malm	713-04801B-E	
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
J. Malm	Jesse Malm	Jesse Malm
DESIGN DATE:	LAST MODIFIED DATE	SHEET:
July 7, 2000	November 23, 2001	6 of 7

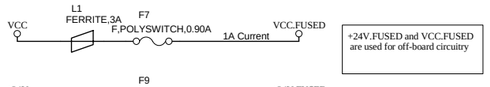
Power Regulation and Filtering

Reset Monitor



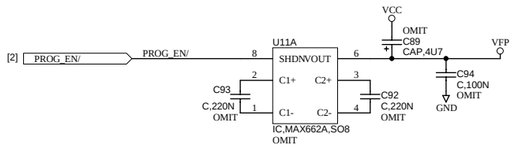
5.00V Analog Reference Voltage

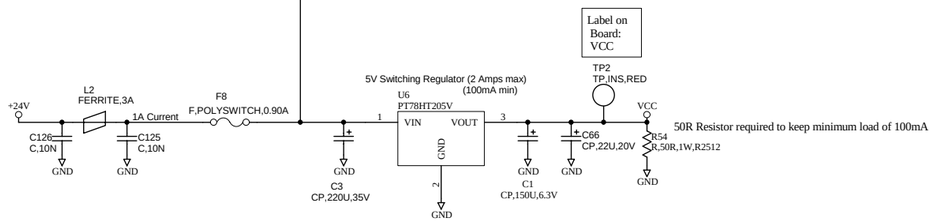




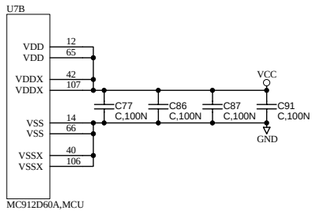
The +12V flash programming supply was required on 10-4801B-B, but is not on 10-4801B-C, due to a new processor which generates the flash programming voltage internally. U11 and associated components (shown inside the dotted boxes) can be removed on the next rev of the PCB.

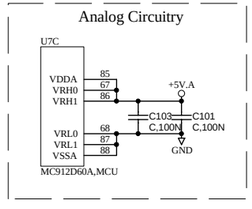
+12V Program Voltage Supply

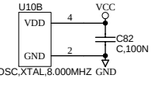




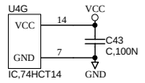
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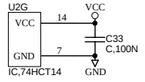


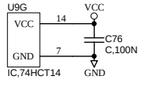


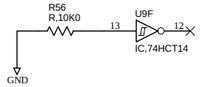


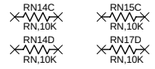
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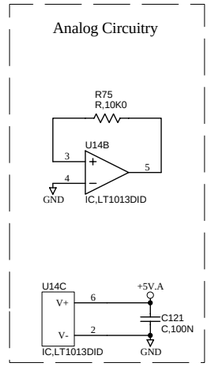




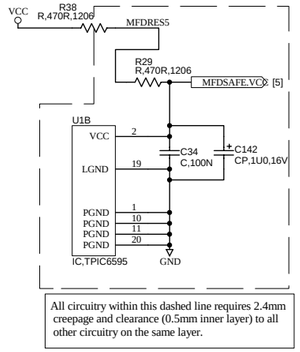




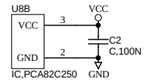
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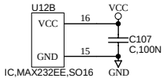


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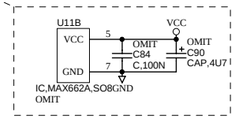


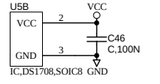
PAGE 6

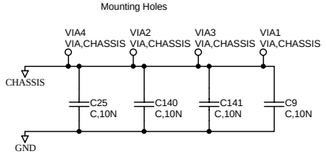




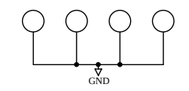
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Label on Board: GND



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LIONEL Schematic
Power Distribution and Filtering
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G:\Electrical\HW\Lionel\10-4801B-E\Eng\713-04801B-C-SD01.ddb - Documents\Page 07 Power_Distrib.sch

DESIGNED BY:	DOCUMENT NUMBER:	LAST ECO:
J. Malm	713-04801B-E	
DRAWN BY:	LAST REVISED BY:	APPROVED BY:
J. Malm	Dean Lowe	Dean Lowe
DESIGN DATE:	LAST MODIFIED DATE:	SHEET:
July 8, 2000	October 31, 2003	7 of 7